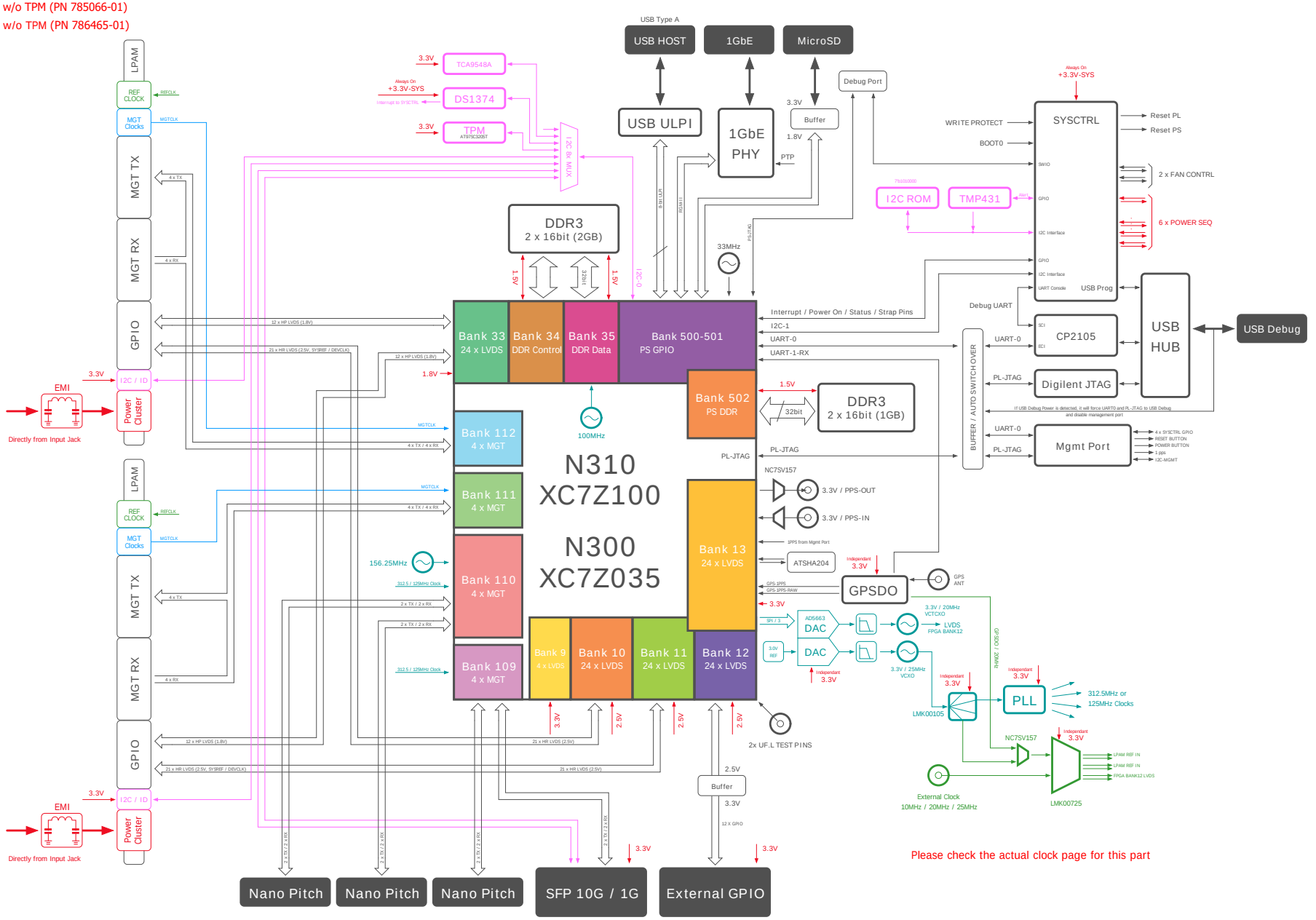
Revisions	
REV	Description

VALID OUTPUT GENERATIONS ARE:
-01L = N310 (PN 785067-01)
-02L = N300 w/o TPM (PN 785066-01)
-03L = N310 w/o TPM (PN 786465-01)



Please check the actual clock page for this part

Design Team		
DRAWN BY		DATE
REVISED BY		DATE
VERIFIED BY		
TECHNICIAN		
ENGINEER		

Ettus Research™ — A National Instruments Company
4600 Patrick Henry Drive
Santa Clara, CA 95054
USA

System Block Diagram
SCH, USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD

SIZE	DOC CODE	DRAWING PROJECT NO	REV
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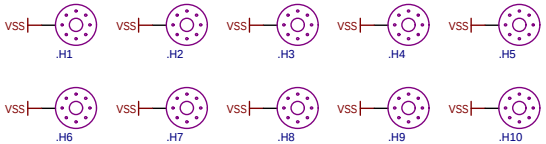
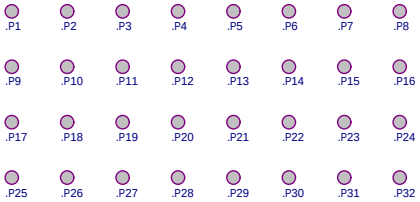
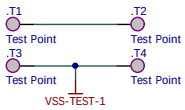
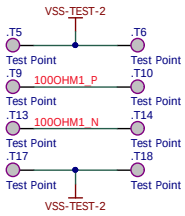
FILE NAME 01_BlockDiagram.SchDoc | DATE 5/21/2018 | SHEET 1 OF 25

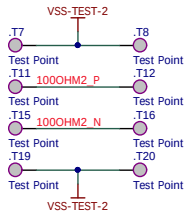
159064F-01

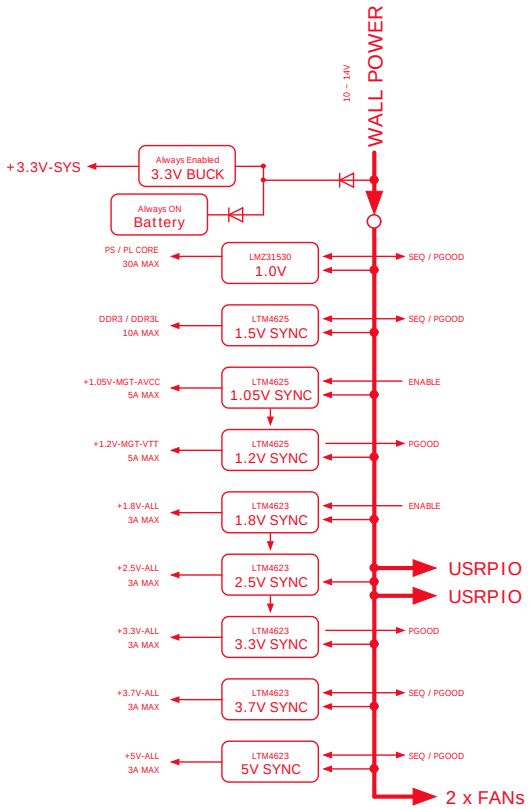






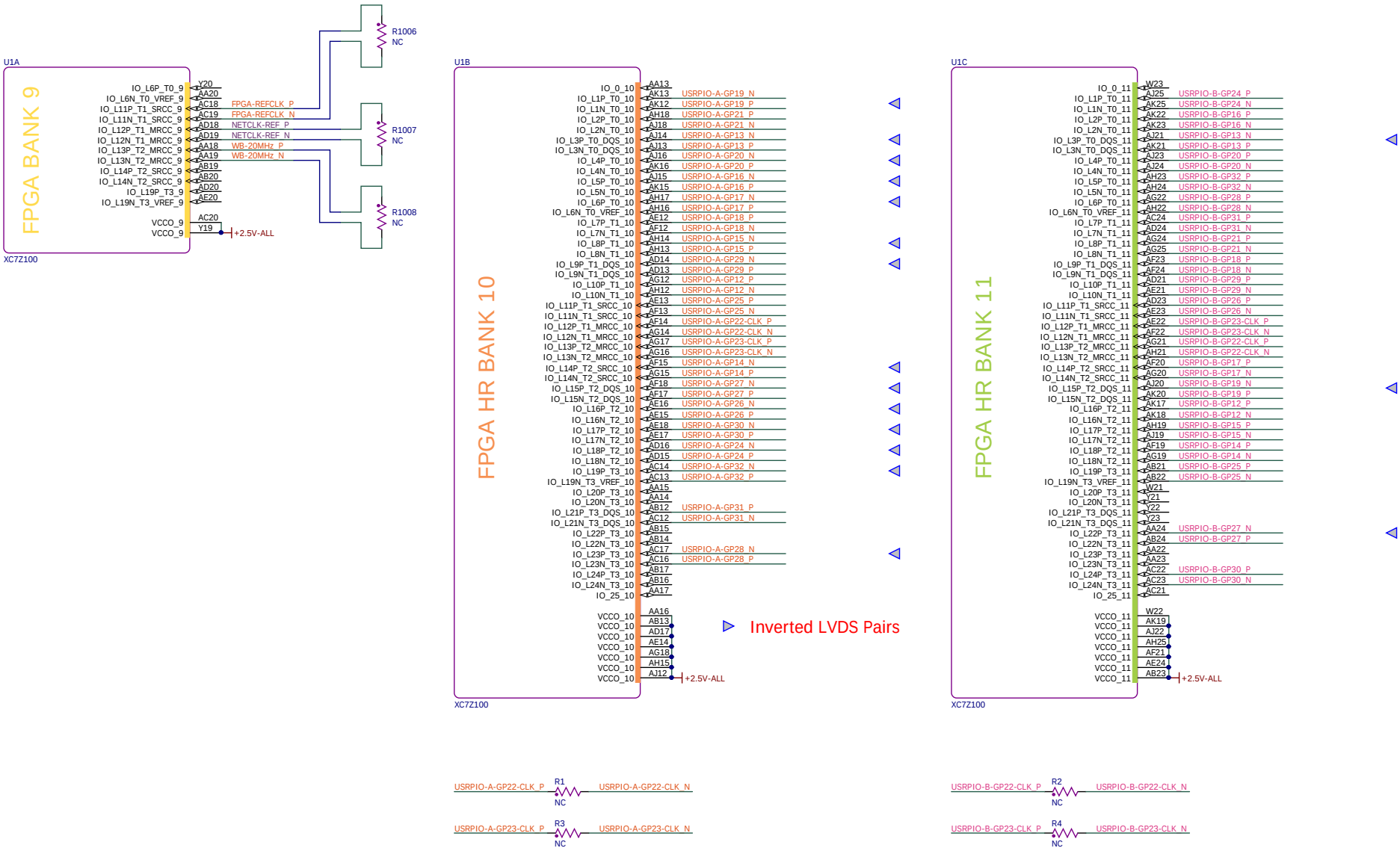






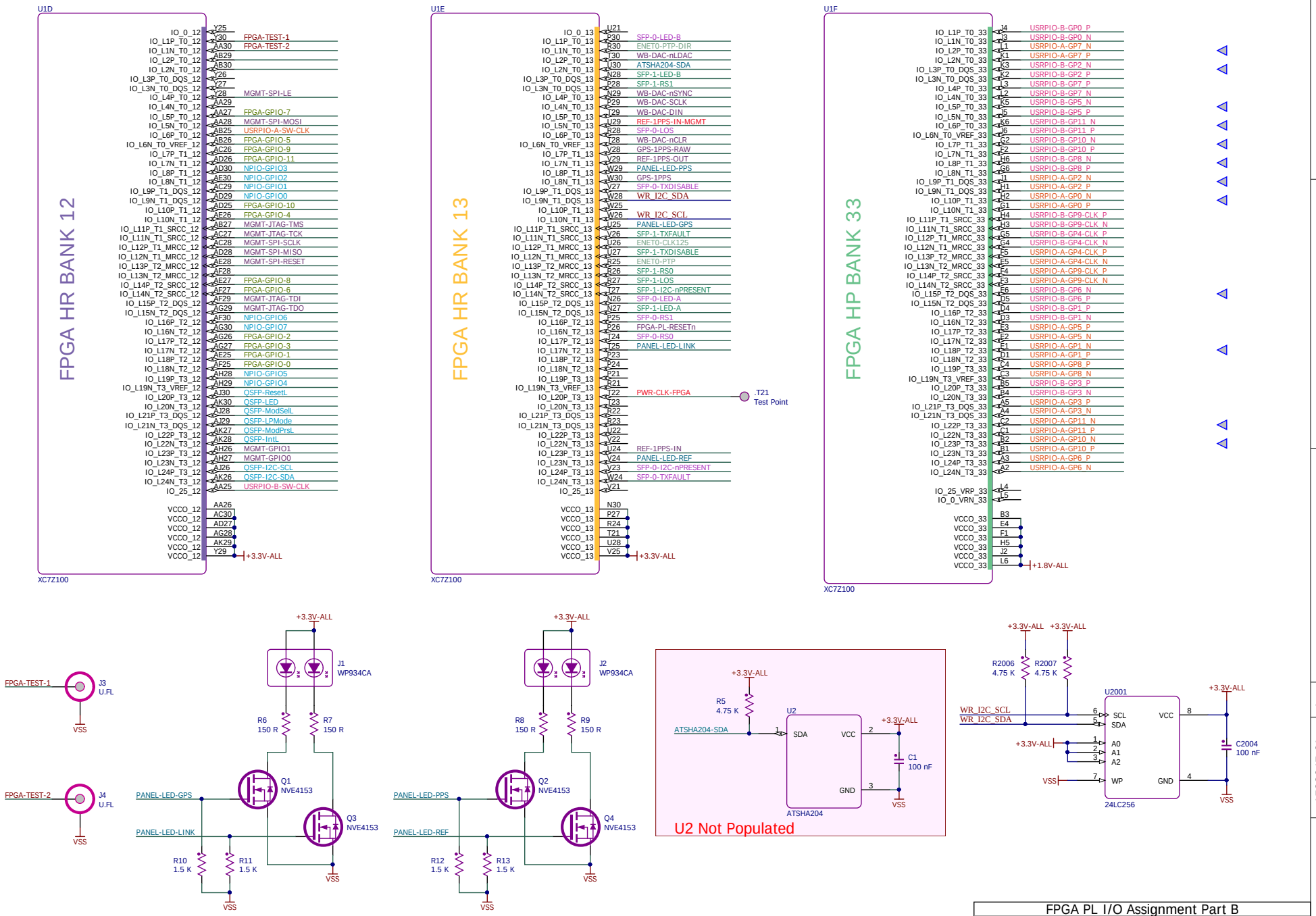
Essential Board Components			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	02_Essential.SchDoc	DATE 5/21/2018	SHEET 2 OF 25

159064F-01

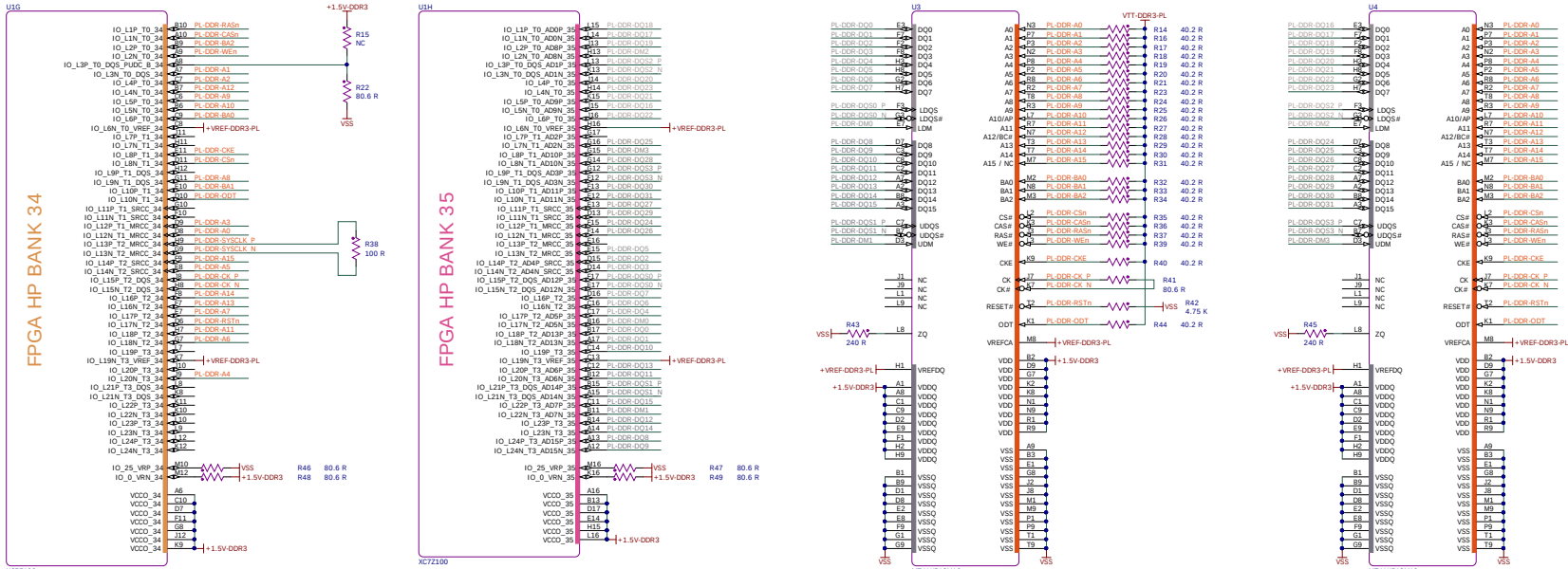


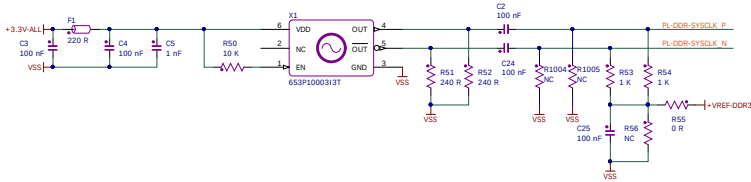
FPGA PL I/O Assignment Part A			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 03_FPGA_PL_IO_A.SchDoc		DATE: 5/21/2018	SHEET 3 OF 25

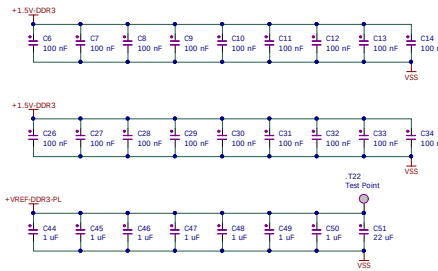
159064F-01

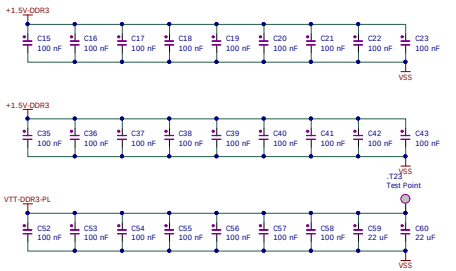


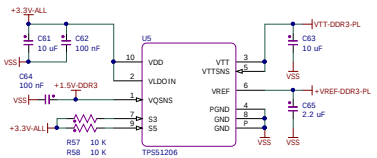
FPGA PL I/O Assignment Part B			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	04_FPGA_PL_IO_B.SchDoc	DATE 5/21/2018	SHEET 4 OF 25





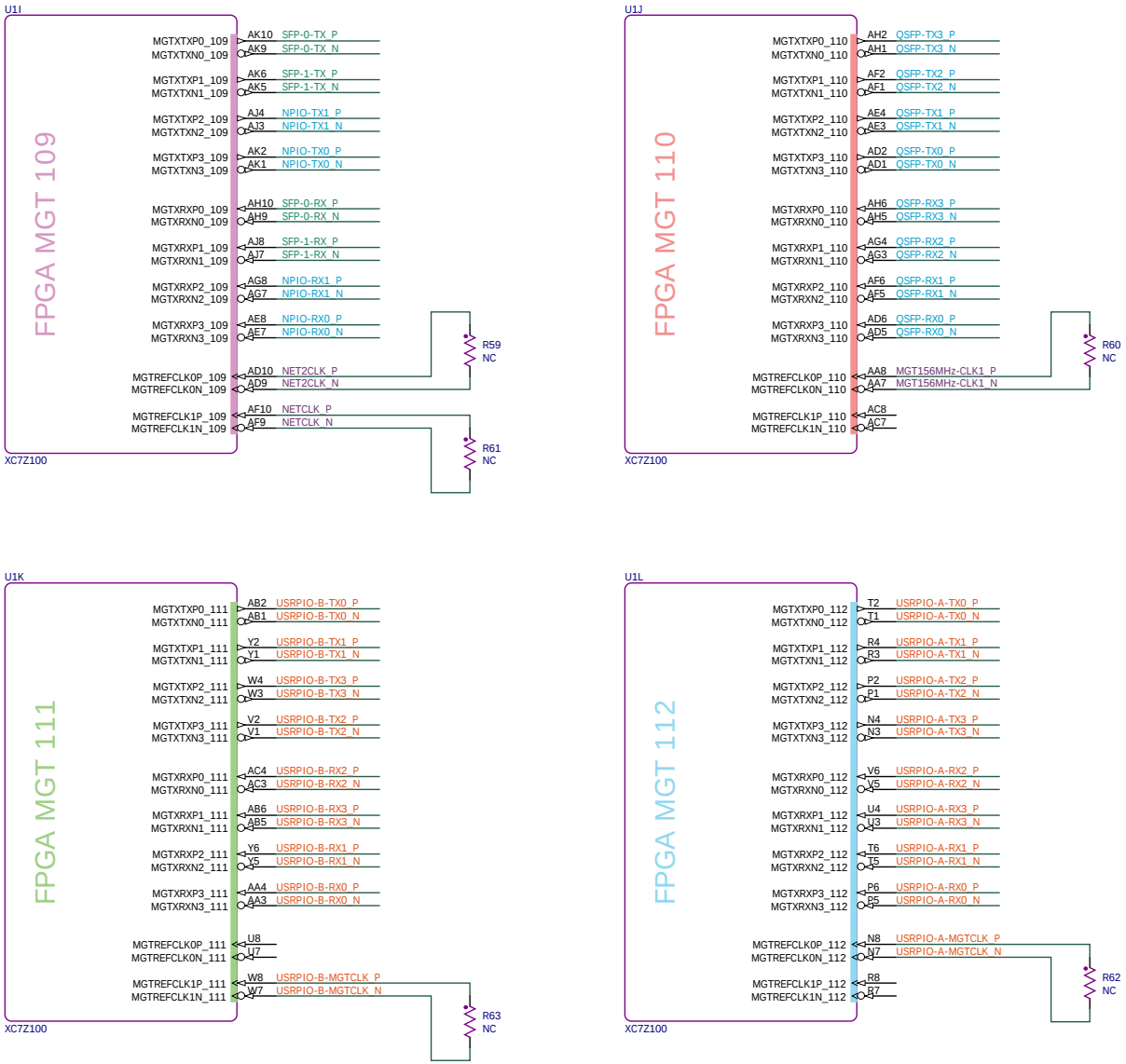






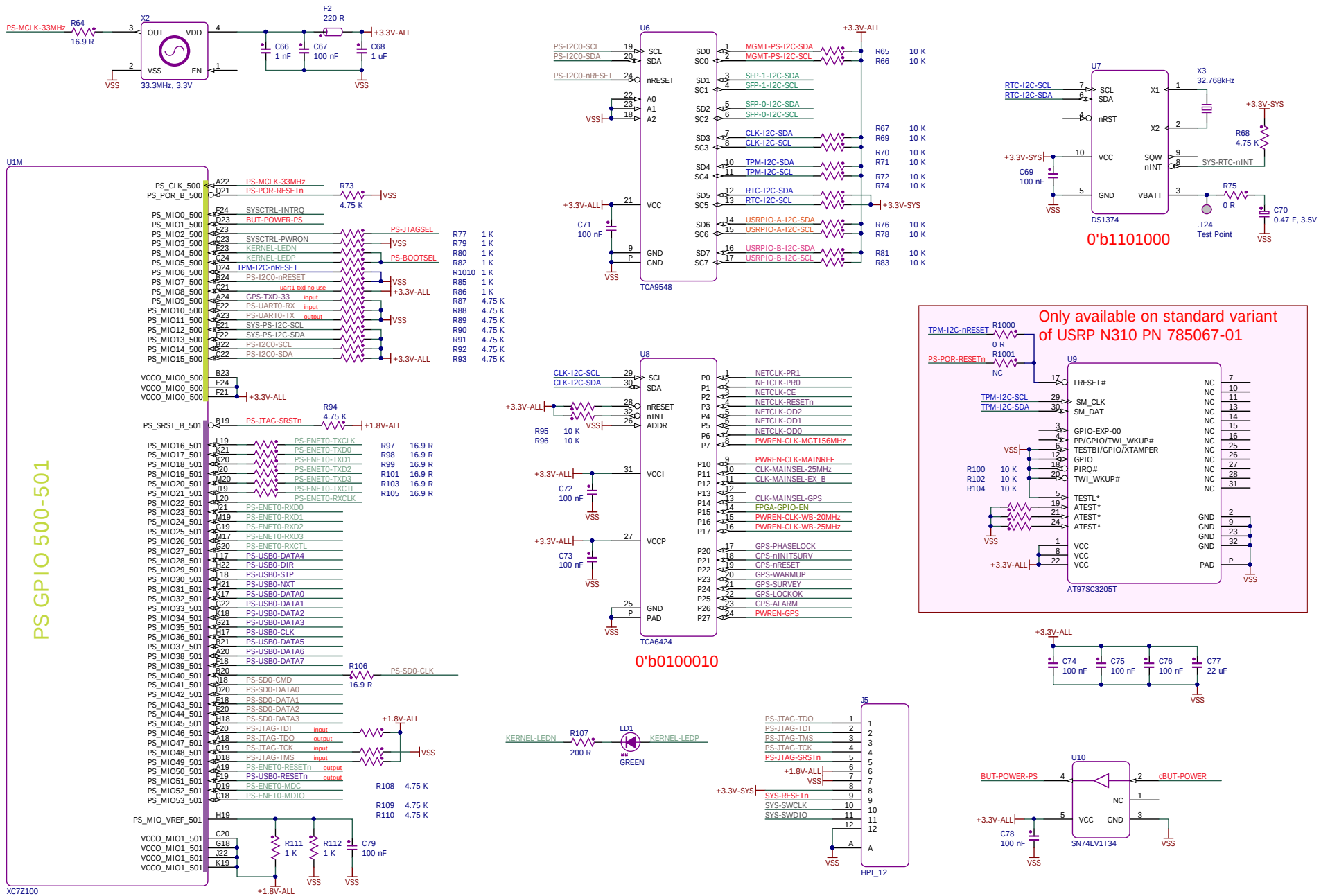
FPGA PL DDR3 Memory			
SCH, USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
D	7U296	159064F-01	1
FILE NAME	05_FPGA_PL_DDR.SchDoc	DATE 5/21/2018	SHEET 5 OF 25

159064F-01



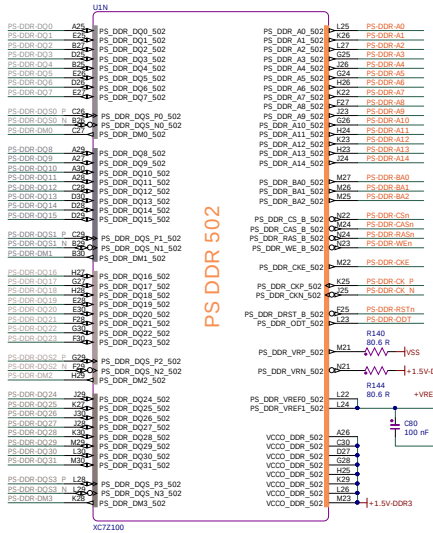
FPGA MGT I/O Assignment			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	06_FPGA_MGT.SchDoc	DATE 5/21/2018	SHEET 6 OF 25

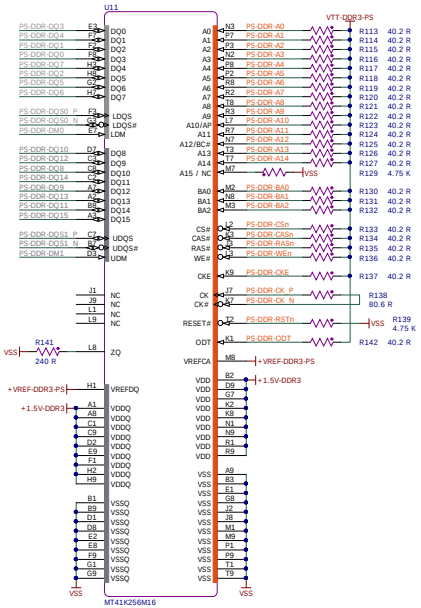
159064F-01

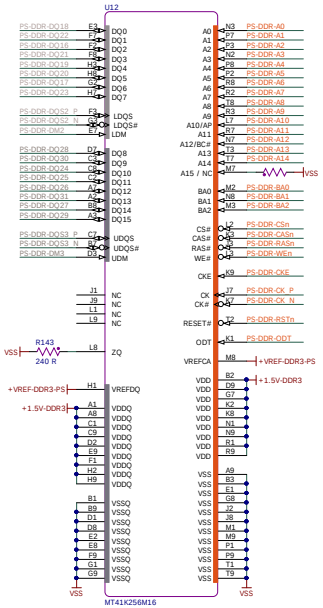


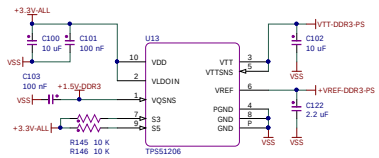
FPGA PS I/O Assignment / I2C / TPM			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 07_FPGA_PS_IO.SchDoc		DATE: 5/21/2018	SHEET 7 OF 25

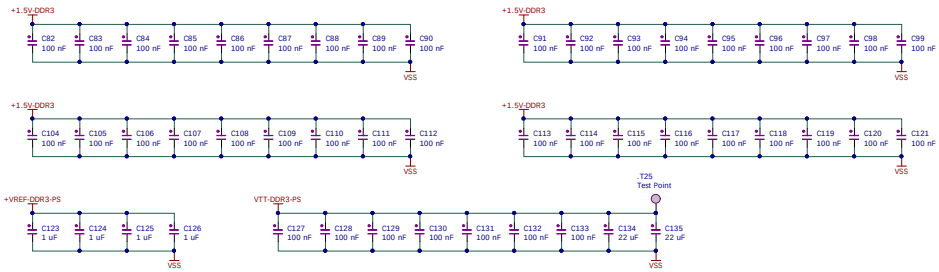
159064F-01



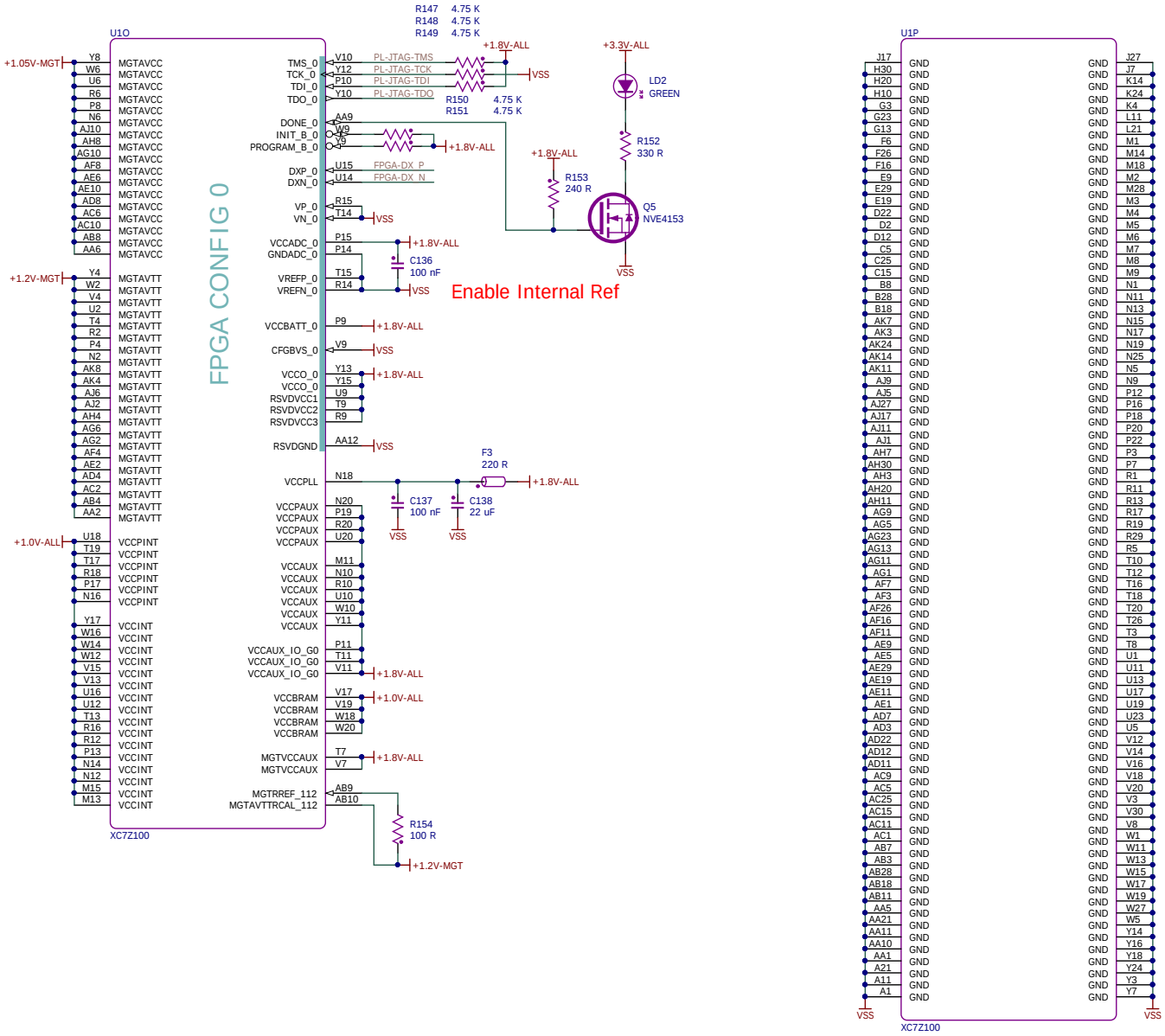






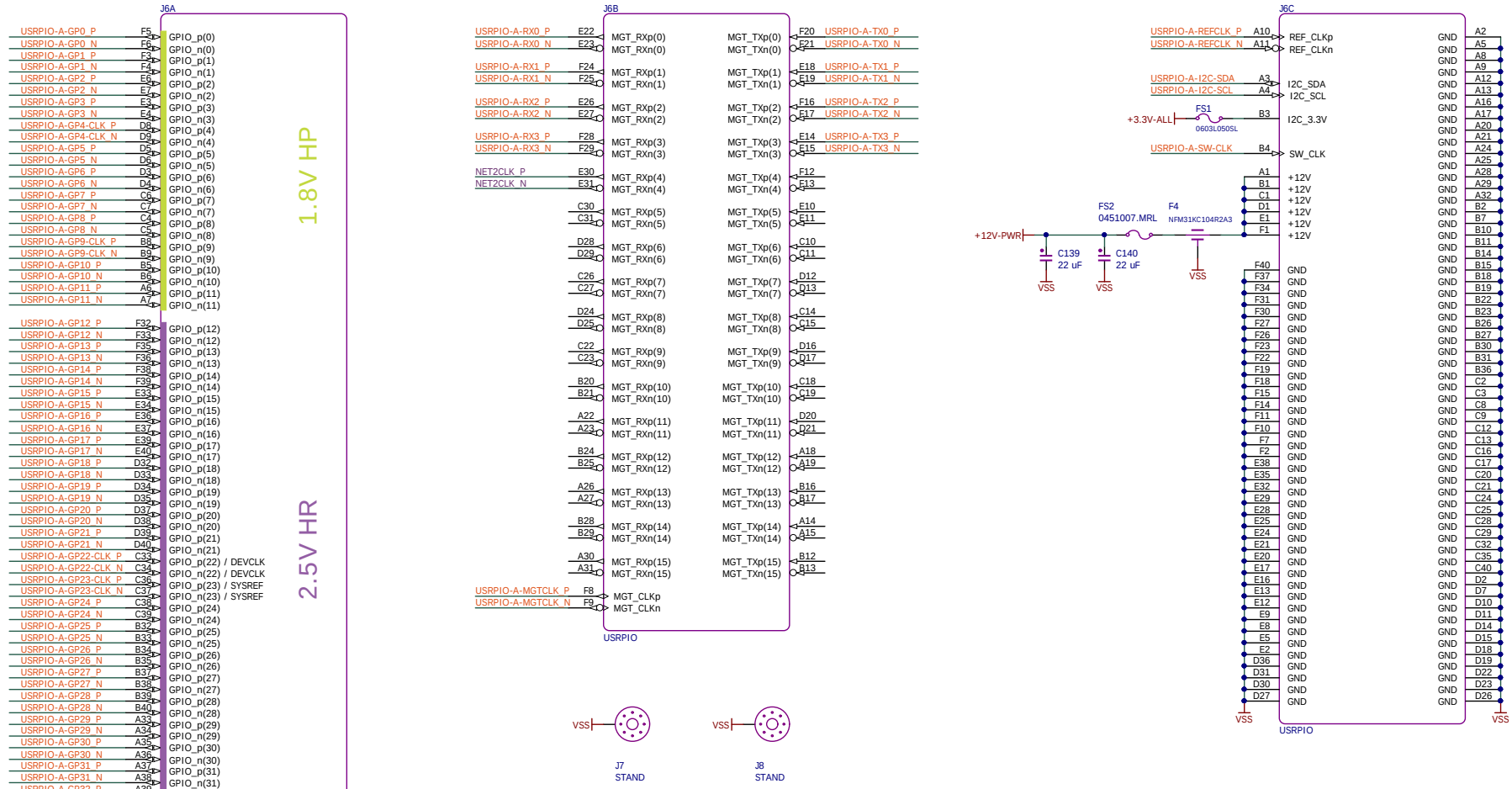


FPGA PS DDR3 Memory			
SCH, USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
D	7U296	159064F-01	1
FILE NAME	08_FPGA_PS_DDR.SchDoc	DATE 5/21/2018	SHEET 8 OF 25



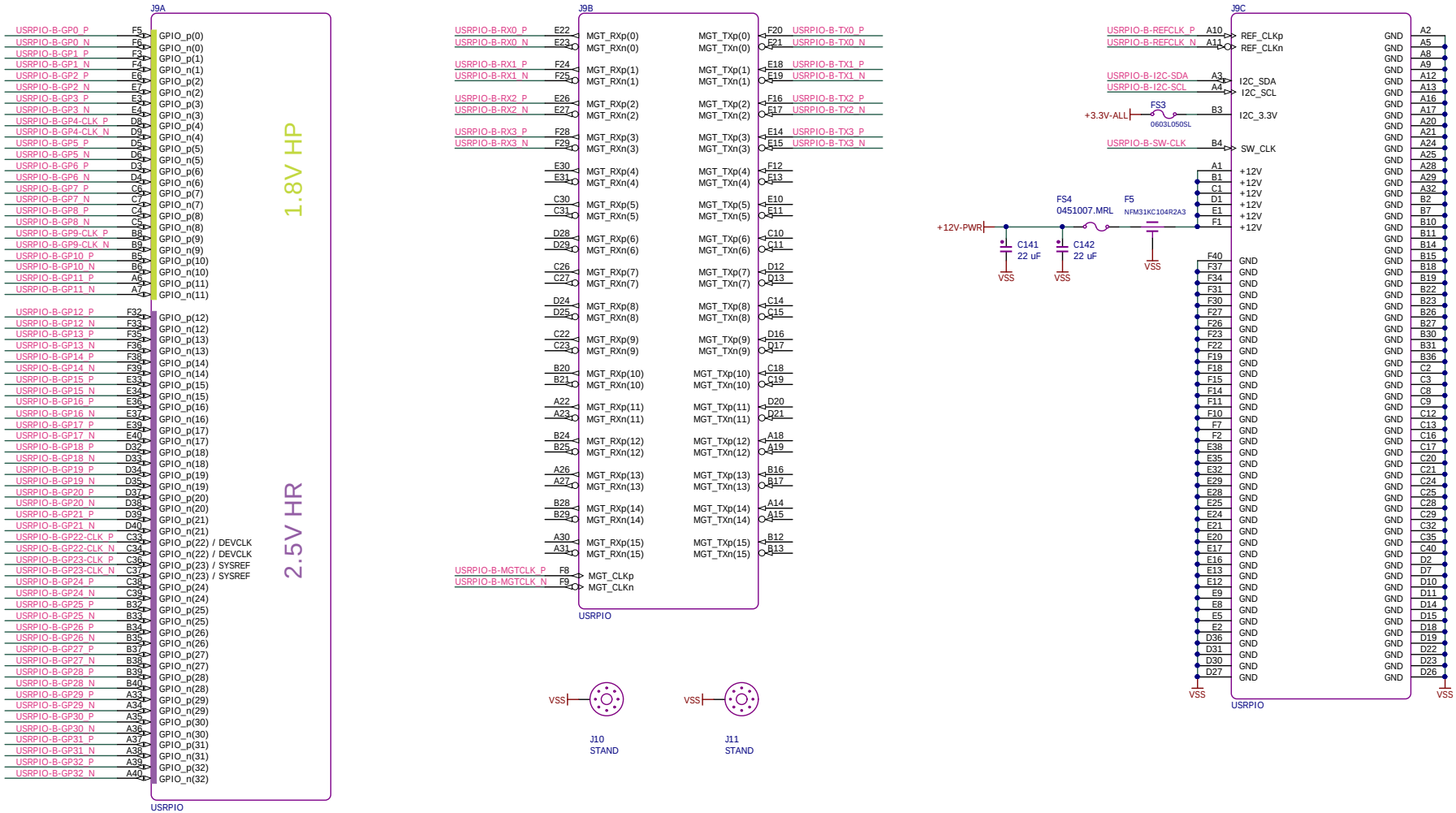
FPGA Power and Configuration			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	09_FPGA_Config.SchDoc	DATE 5/21/2018	SHEET 9 OF 25

159064F-01



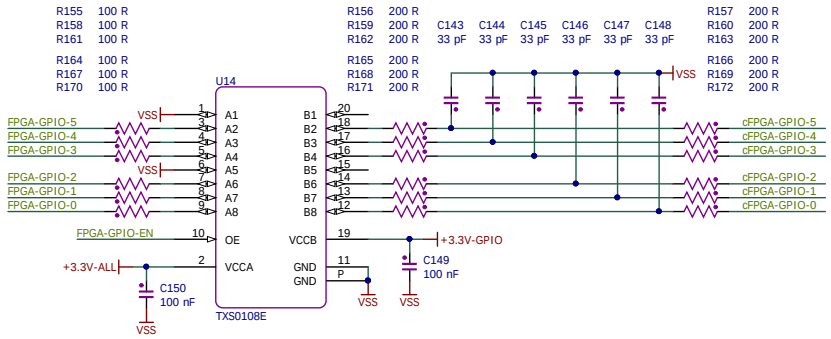
USRPIO Channel A			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	10_USRPIO_A.SchDoc	DATE 5/21/2018	SHEET 10 OF 25

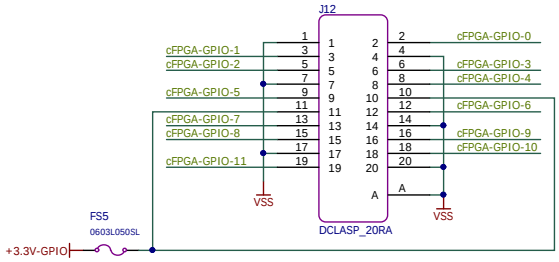
159064F-01

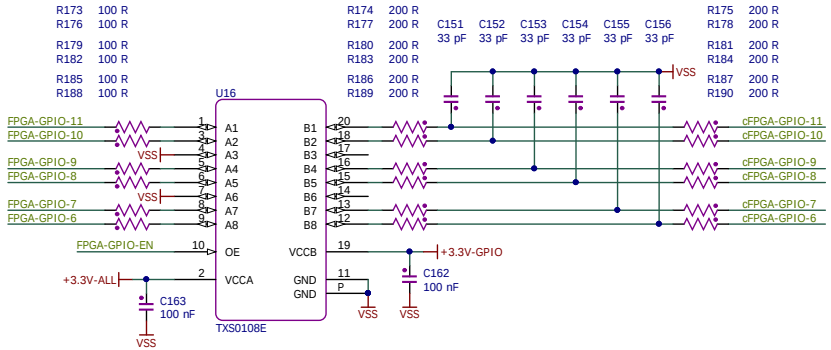


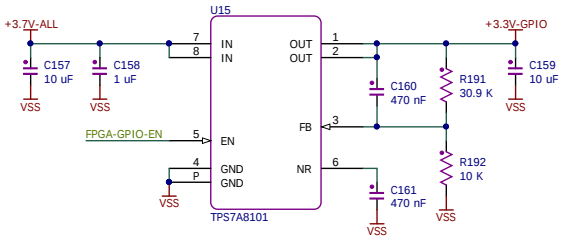
USRPIO Channel B			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	11_USRPIO_B.SchDoc	DATE 5/21/2018	SHEET 11 OF 25

159064F-01









GPIO Interface			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
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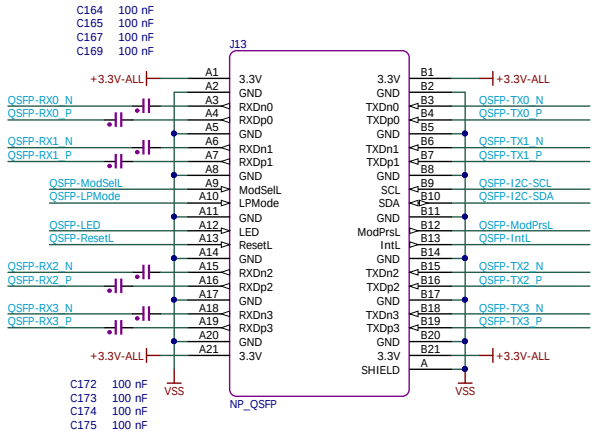
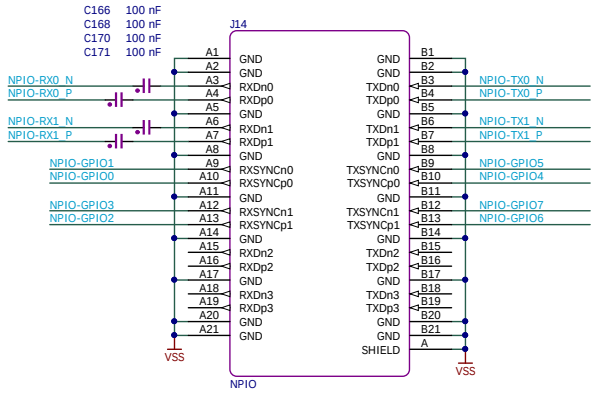
FILE NAME	12_GPIO.SchDoc	DATE 5/21/2018	SHEET 12 OF 25

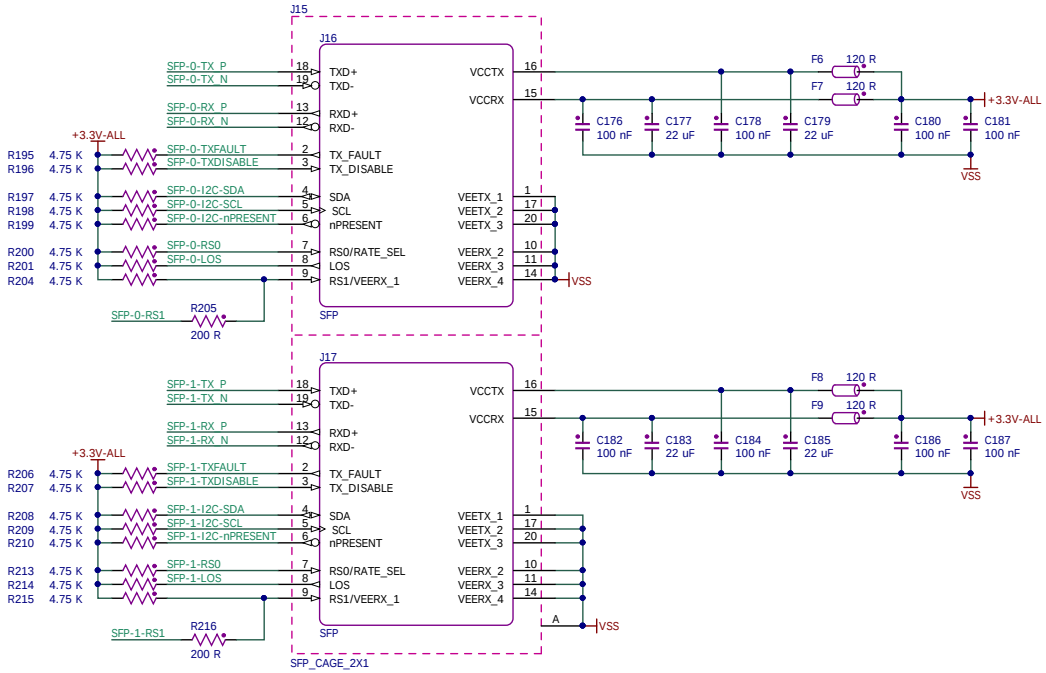
159064F-01

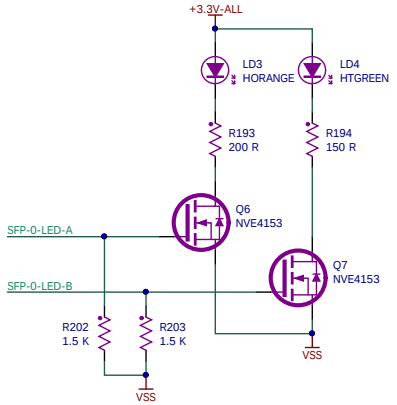


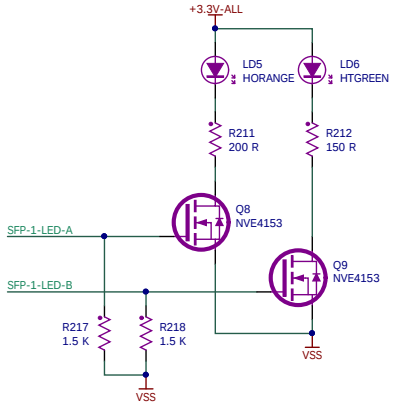


Nano pitch IO Interface			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 13_NPIO.SchDoc		DATE: 5/21/2018	SHEET 13 OF 25

159064F-01







SFP+ Interface

USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD

SIZE	DOC CODE	DRAWING PROJECT NO	REV
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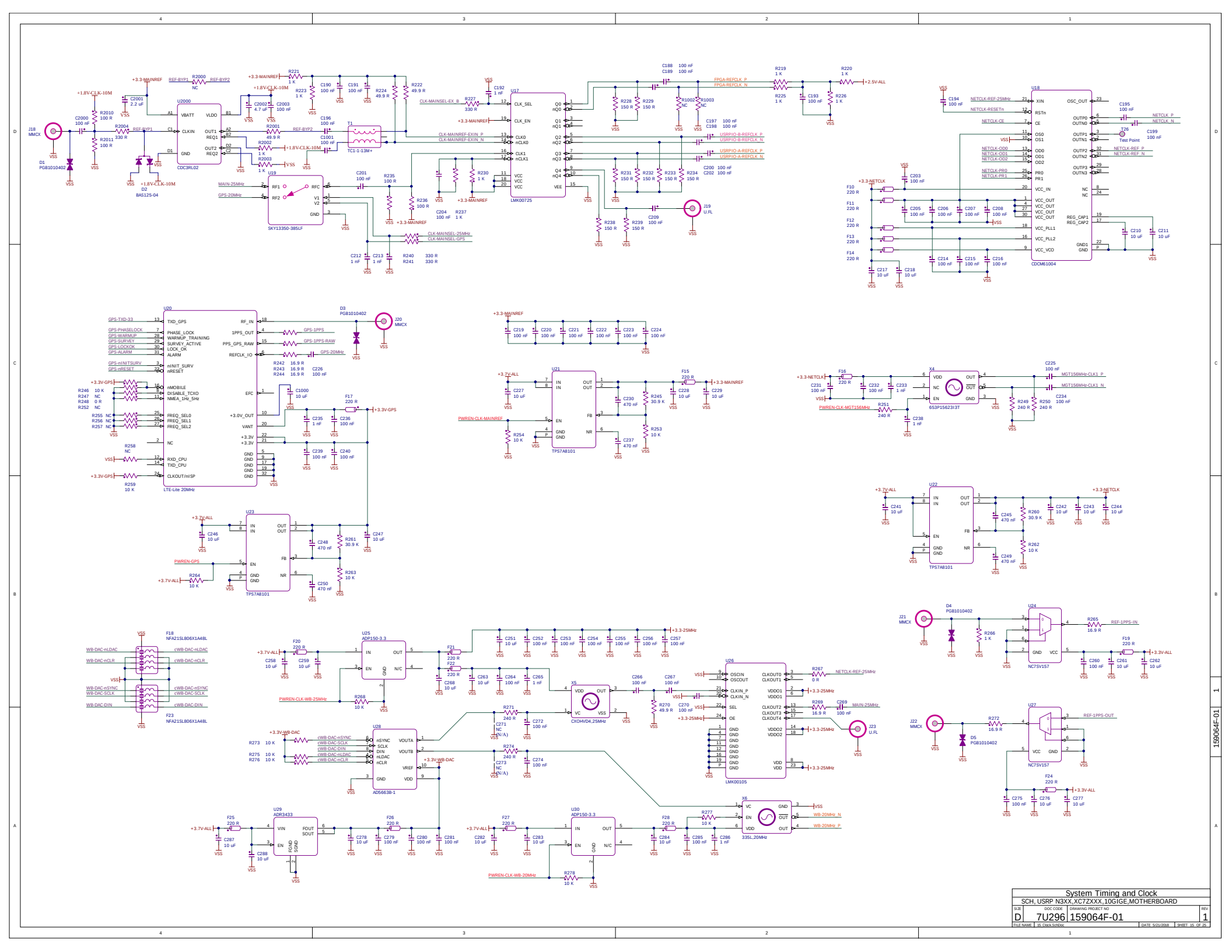
FILE NAME	DATE	SHEET
14_SFP.SchDoc	5/21/2018	14 OF 25

159064F-01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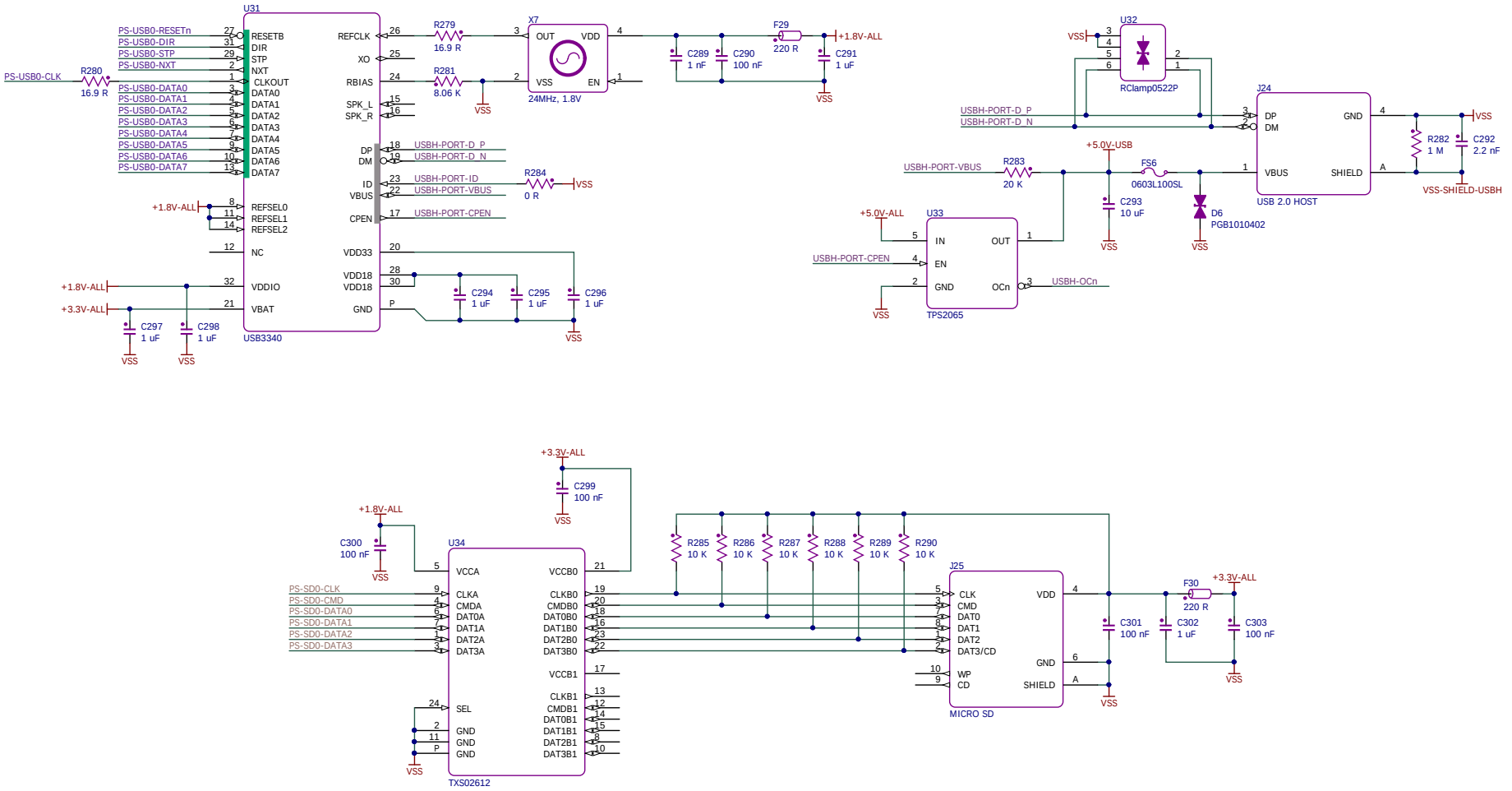
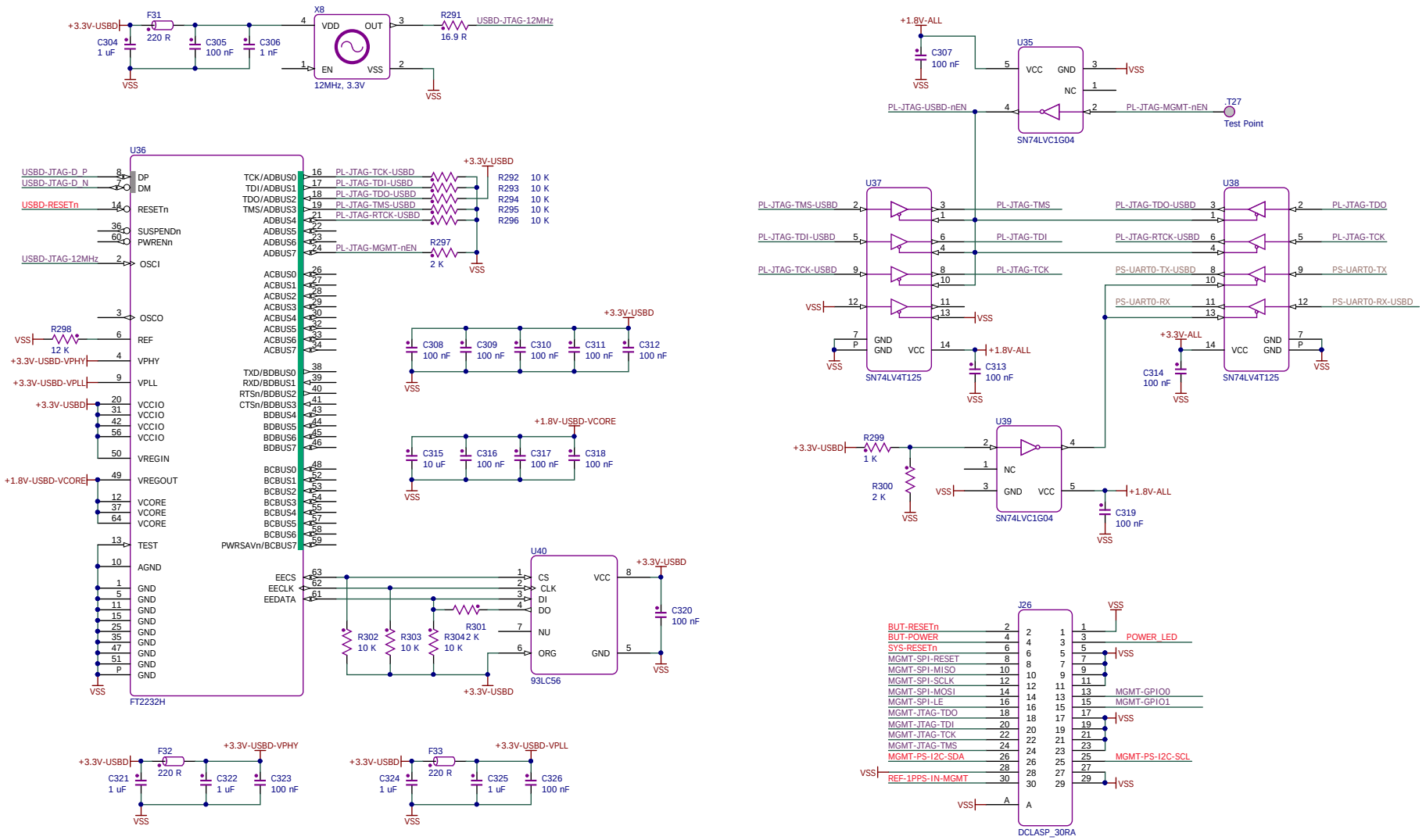
CDC3RL02
U17
LMK00725
U18
CDCM61004
U19
SKY13350-385LF
U20
LTE-Lite 20MHz
U21
TPS7A8101
U22
TPS7A8101
U23
TPS7A8101
U24
NC7SV157
U25
ADP150-3.3
U26
LMK00105
U27
NC7SV157
U28
AD5663B-1
U29
ADR3433
U30
ADP150-3.3
X4
653P156231ST
X5
CXOHVD4,25MHz
X6
335L,20MHz
T1
TC1-1-13M+
D1
PGB1010402
D2
BAS125-04
D3
PGB1010402
D4
PGB1010402
D5
PGB1010402
J18
MMCX
J19
U.FL
J20
MMCX
J21
MMCX
J22
MMCX
J23
U.FL
T26
Test Point
+1.8V-CLK-10M
+3.3-MAINREF
+2.5V-ALL
+3.3V-NETCLK
+3.3V-GPS
+3.7V-ALL
+3.3-WB-DAC
+3.3-25MHz
MAIN-25MHz
GPS-20MHz
NETCLK-REF-25MHz
NETCLK-RESETn
NETCLK-CE
NETCLK-OD0
NETCLK-OD1
NETCLK-OD2
NETCLK-PR0
NETCLK-PR1
FPGA-REFCLK_P
FPGA-REFCLK_N
USRPIO-B-REFCLK_P
USRPIO-B-REFCLK_N
USRPIO-A-REFCLK_P
USRPIO-A-REFCLK_N
CLK-MAINSEL-EX_B
CLK-MAINREF-EXIN_P
CLK-MAINREF-EXIN_N
CLK-MAINSEL-25MHz
CLK-MAINSEL-GPS
MGT156MHz-CLK1_P
MGT156MHz-CLK1_N
PWREN-CLK-MGT156MHz
PWREN-CLK-MAINREF
PWREN-GPS
PWREN-CLK-WB-25MHz
PWREN-CLK-WB-20MHz
WB-DAC-nLDAC
WB-DAC-nCLR
WB-DAC-nSYNC
WB-DAC-SCLK
WB-DAC-DIN
WB-20MHz_N
WB-20MHz_P
REF-1PPS-IN
REF-1PPS-OUT
GPS-TXD-33
GPS-PHASELOCK
GPS-WARMUP
GPS-SURVEY
GPS-LOCKOK
GPS-ALARM
GPS-nINITSURV
GPS-nRESET
GPS-1PPS
GPS-1PPS-RAW
GPS-20MHz
REF-BYP1
REF-BYP2
System Timing and Clock
SCH, USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD
SIZE D
DOC CODE 7U296
DRAWING PROJECT NO 159064F-01
REV 1
FILE NAME 15_Clock.SchDoc
DATE 5/21/2018
SHEET 15 OF 25

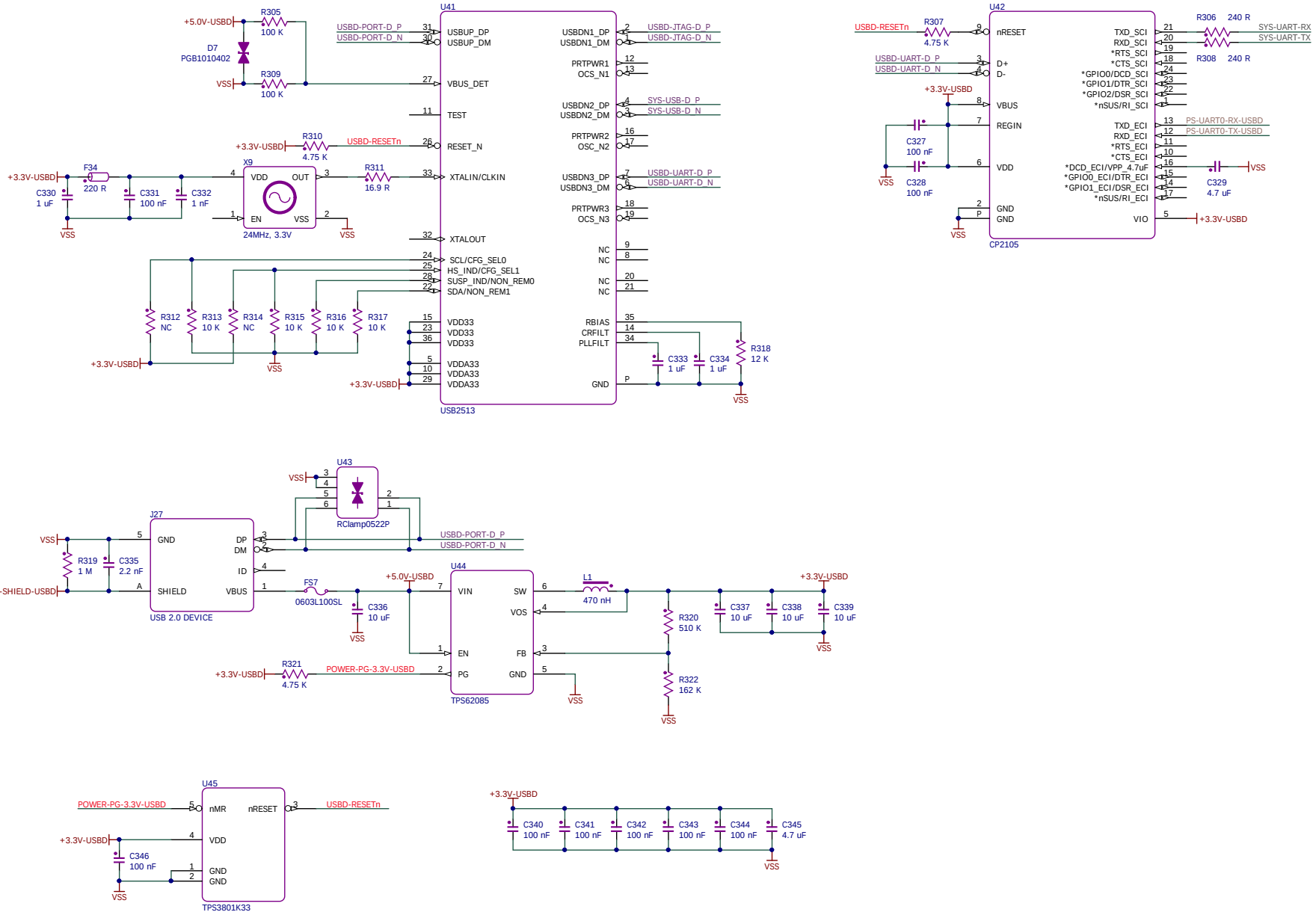


USB 2.0 Host / MicroSD			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 16_USBHost_MicroSD.SchDoc		DATE: 5/21/2018	SHEET 16 OF 25

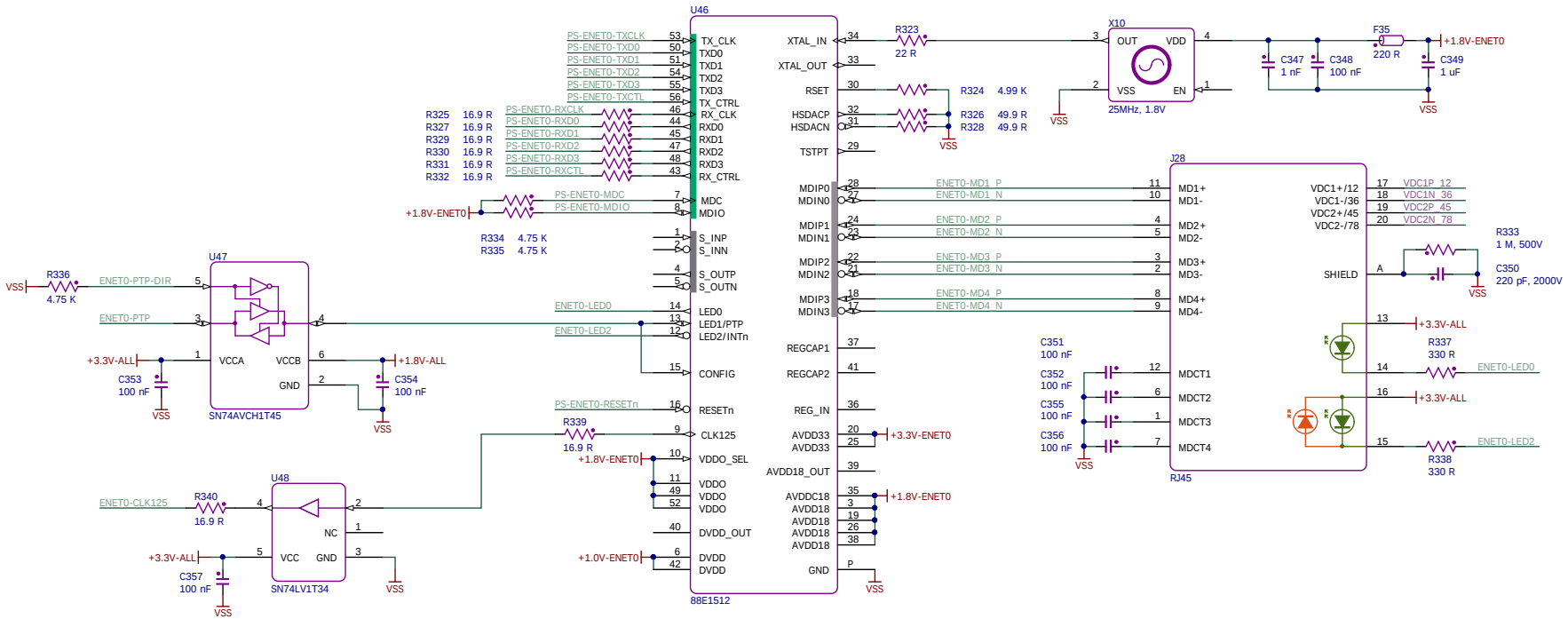
159064F-01



USB JTAG and USB UART for Debug			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	17_USB_Debug.SchDoc	DATE 5/21/2018	SHEET 17 OF 25

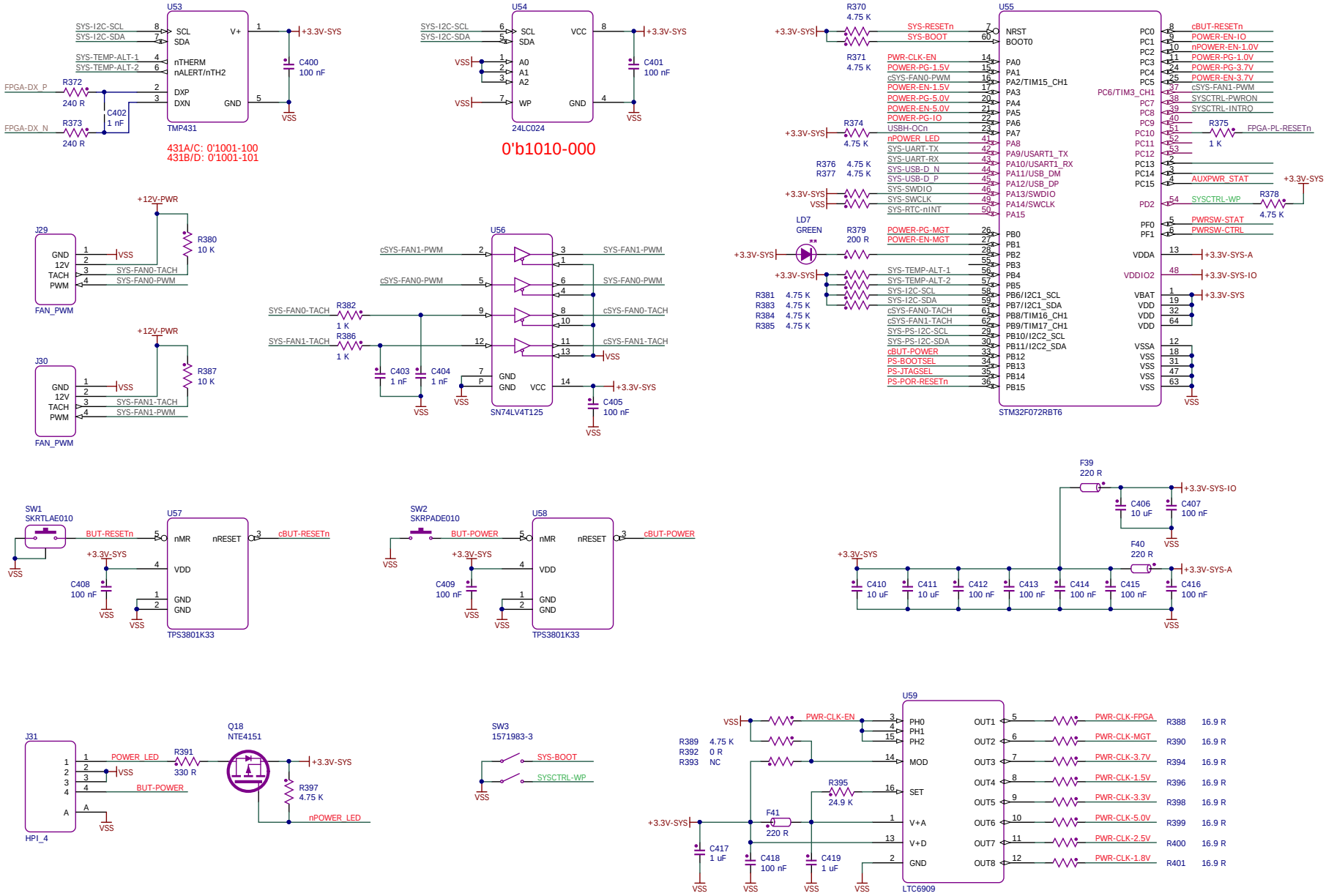


USB 2.0 Hub for Debug Interface			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	18_USB_Hub.SchDoc	DATE 5/21/2018	SHEET 18 OF 25

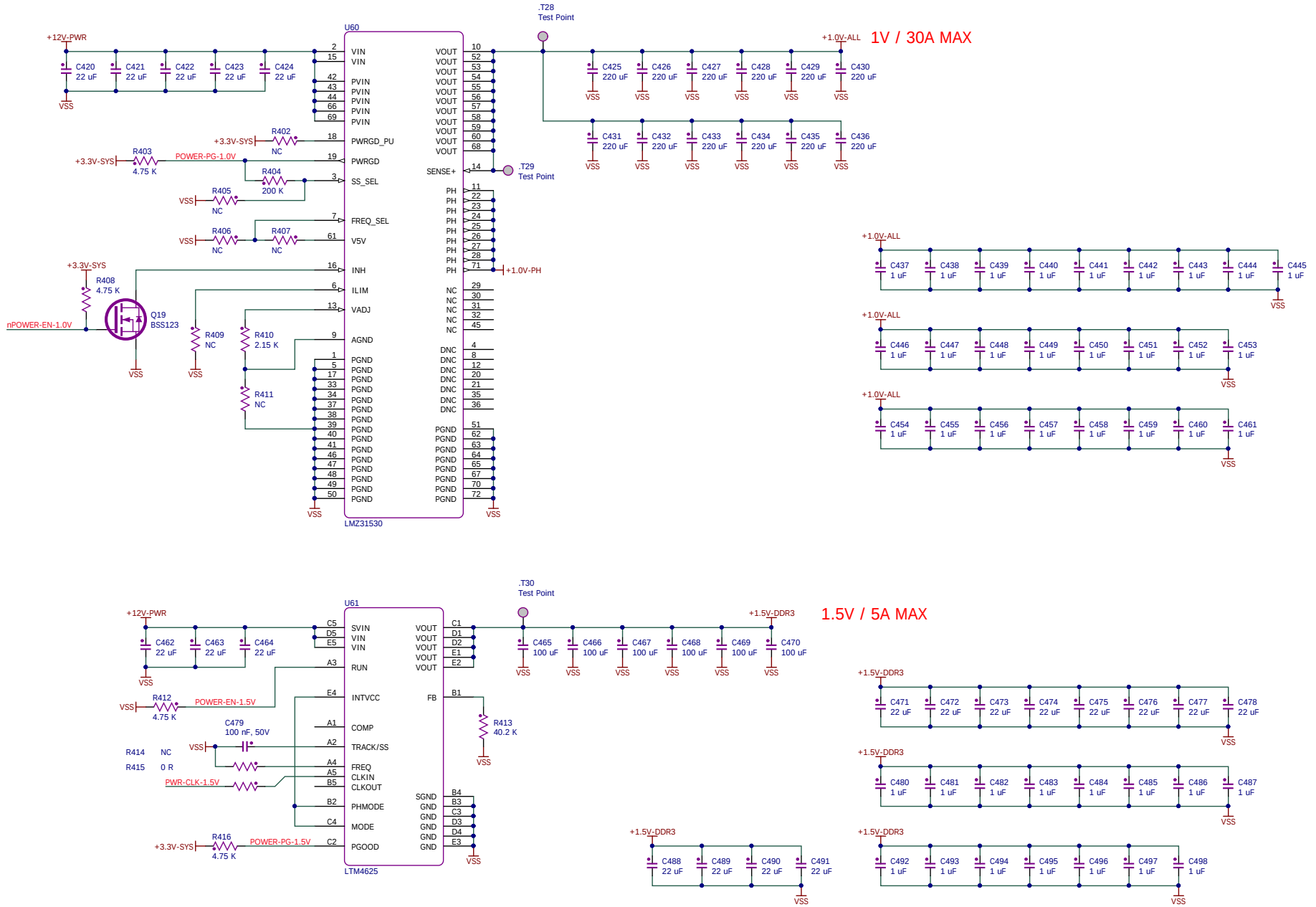


GbE Ethernet Controller and RJ45 Connector			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	19_Ethernet_Controller.SchDoc	DATE 5/21/2018	SHEET 19 OF 25

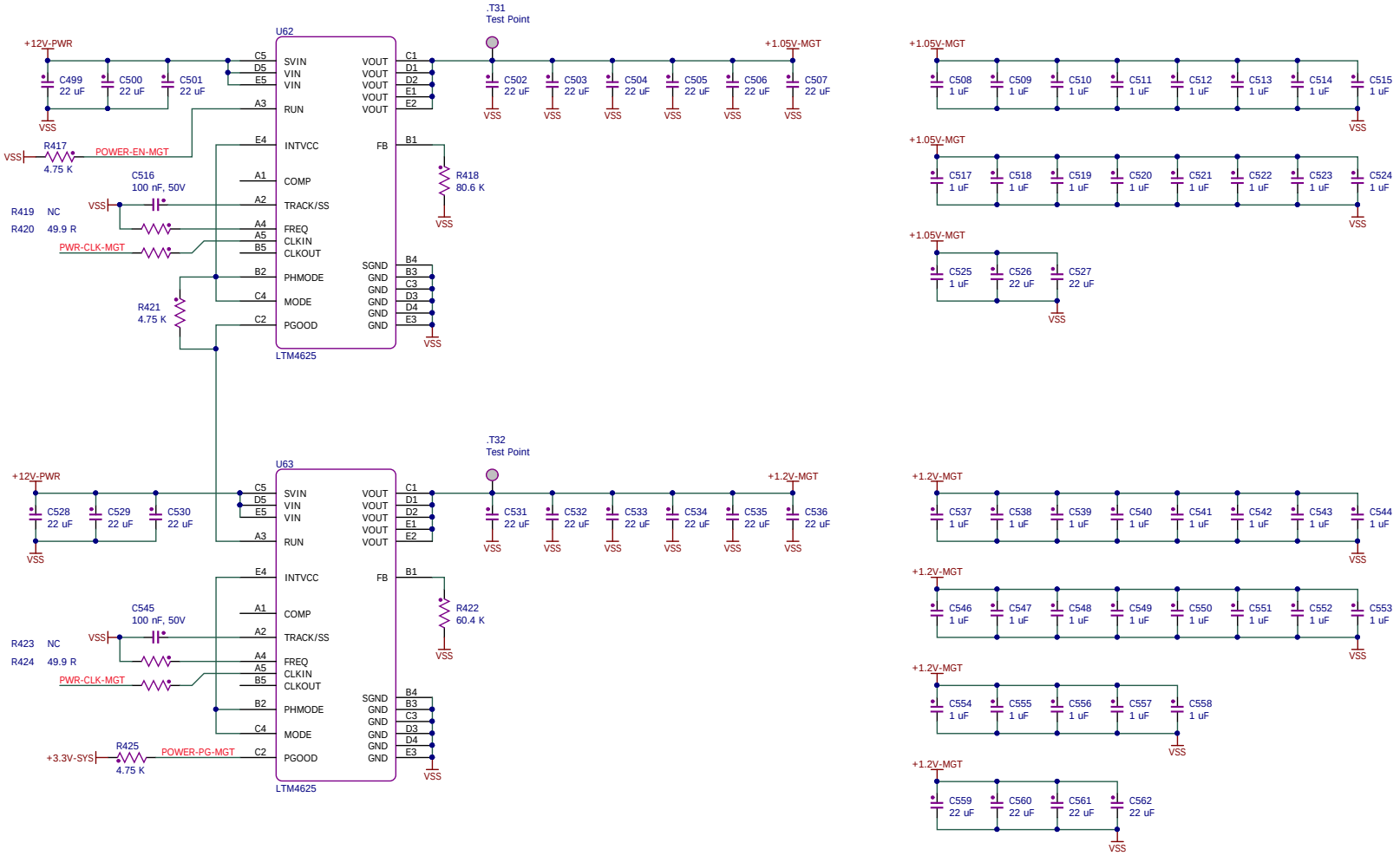
159064F-01



System Controller			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	21_SYSCTRL.SchDoc	DATE 5/21/2018	SHEET 21 OF 25

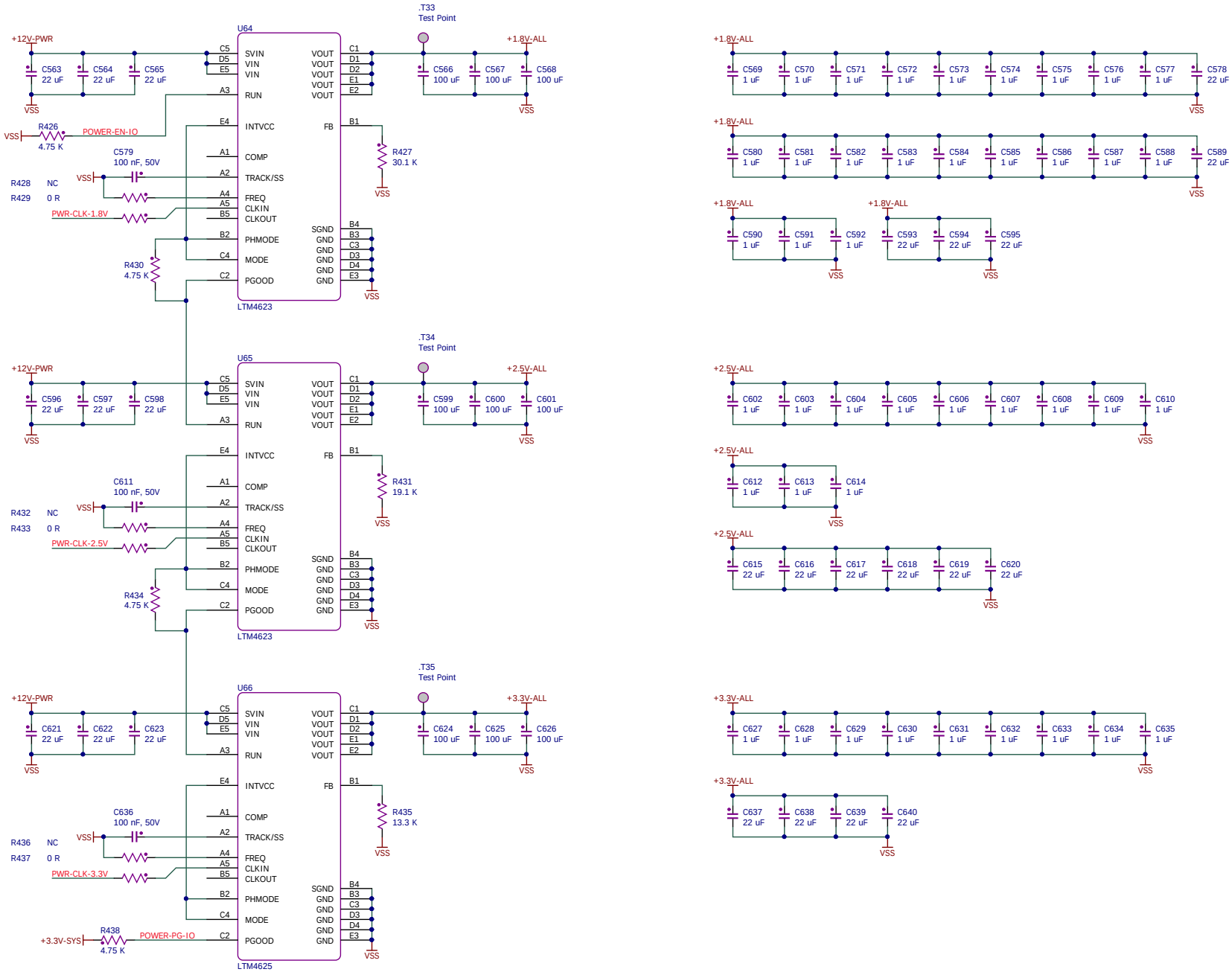


Power Converter Part A			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	22_POWER_A.SchDoc	DATE 5/21/2018	SHEET 22 OF 25

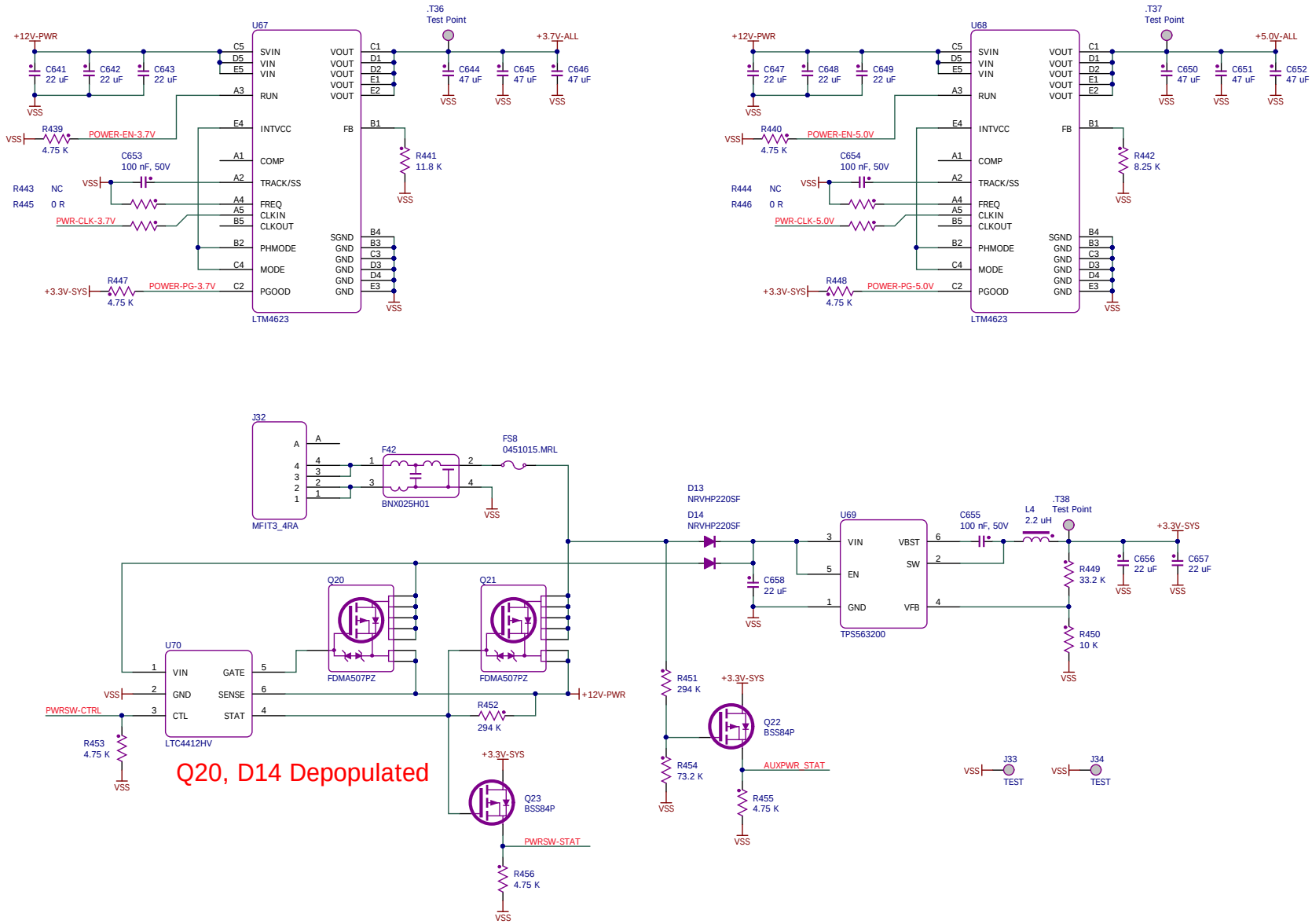


Power Converter Part B			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 23_POWER_B.SchDoc		DATE: 5/21/2018	SHEET 23 OF 25

159064F-01



Power Converter Part C			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 24_POWER_C.SchDoc		DATE: 5/21/2018	SHEET 24 OF 25



Power Converter Part D			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	25_POWER_D.SchDoc	DATE 5/21/2018	SHEET 25 OF 25