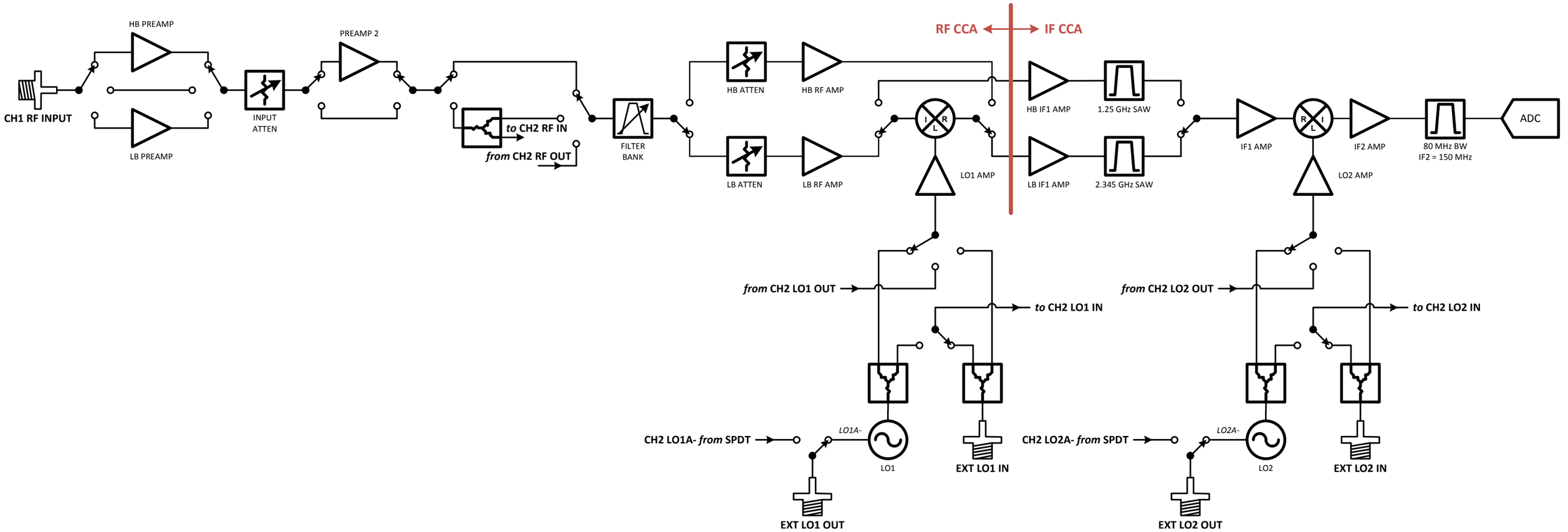
Simplified block diagram for one channel of a two-channel, 10 MHz to 6 GHz superheterodyne daughterboard for X3x0 (80 MHz BW).

Dual LOs per channel utilize ADF5355s and ADF4351s, synchronizable via FPGA I/O lines. Switchable LO input and output ports exist between channels.



NATIONAL INSTRUMENTS	Twin Rx
	Rev B - Simplified