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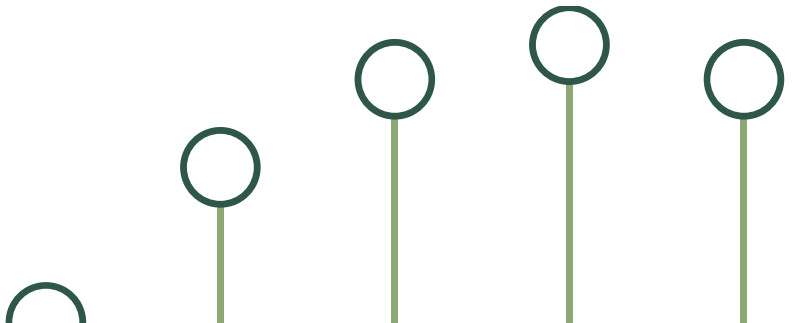
RFNoC™: RF Network on Chip

Martin Braun, Jonathon Pendlum

5/28/2014



Outline

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- Host-based Software Defined Radio
  - Current situation
  - Goal
- RFNoC
  - Architecture overview
- Demo
- Summary

Host-Based SDR – Current Situation

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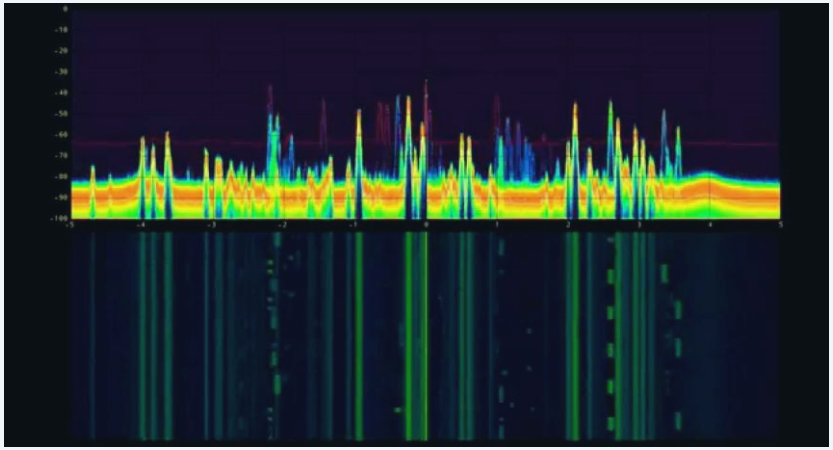
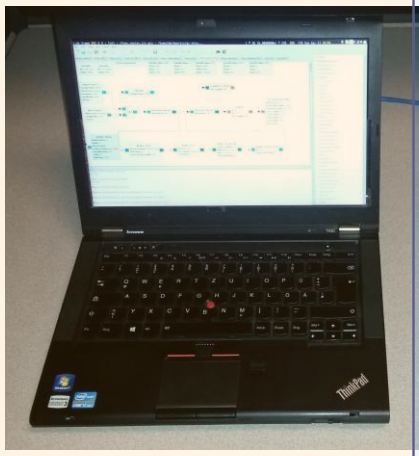
- PC + Flexible RF Hardware + SDR Framework
- Typical SDR frameworks excel at software reconfigurability & composability
- Less true for available hardware

GPU



GPP



FPGA

GNU Radio

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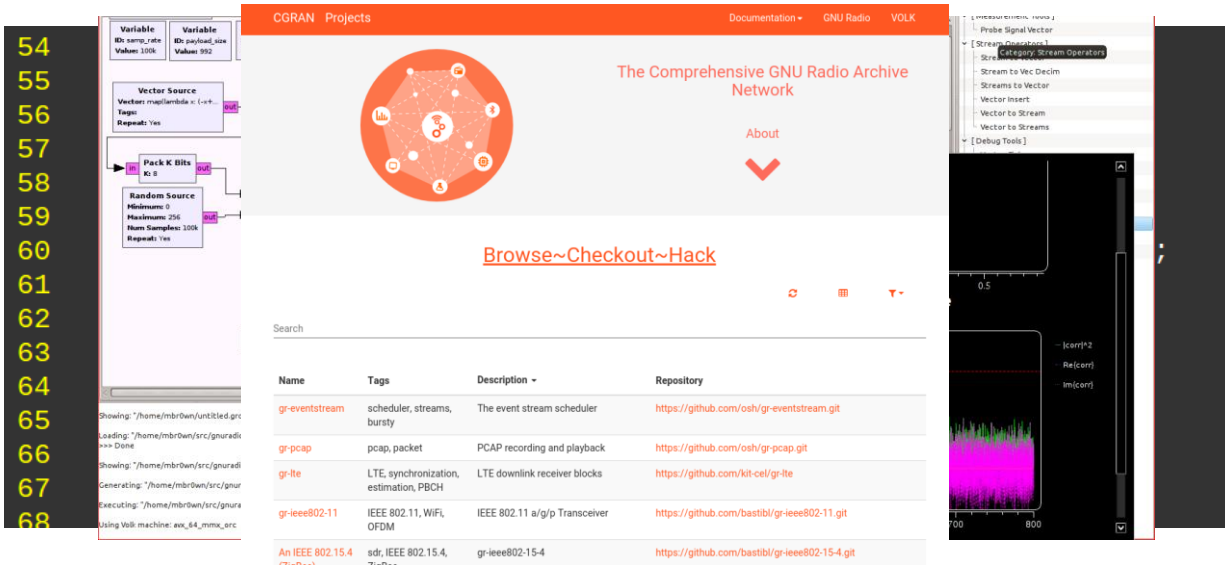
- Most popular DSP/Streaming Framework in the Free Software Universe
  - C++/VOLK for fast DSP -- Python for easy scripting
  - Graphical Development Tool
  - Extensible, many contributions



- RFNoC: Not tied to any particular framework

USRP: A White Box?

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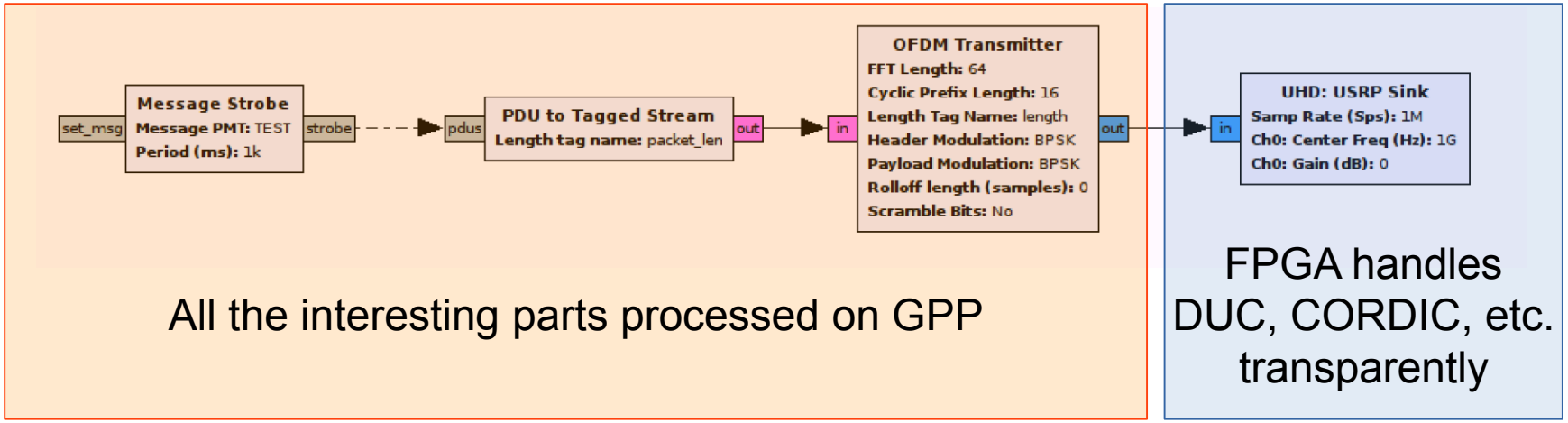
- Simple OFDM Transmitter Development:



- Entire Hardware stack is treated like a reprogrammable ASIC, Features are used as-is

Open the Box!

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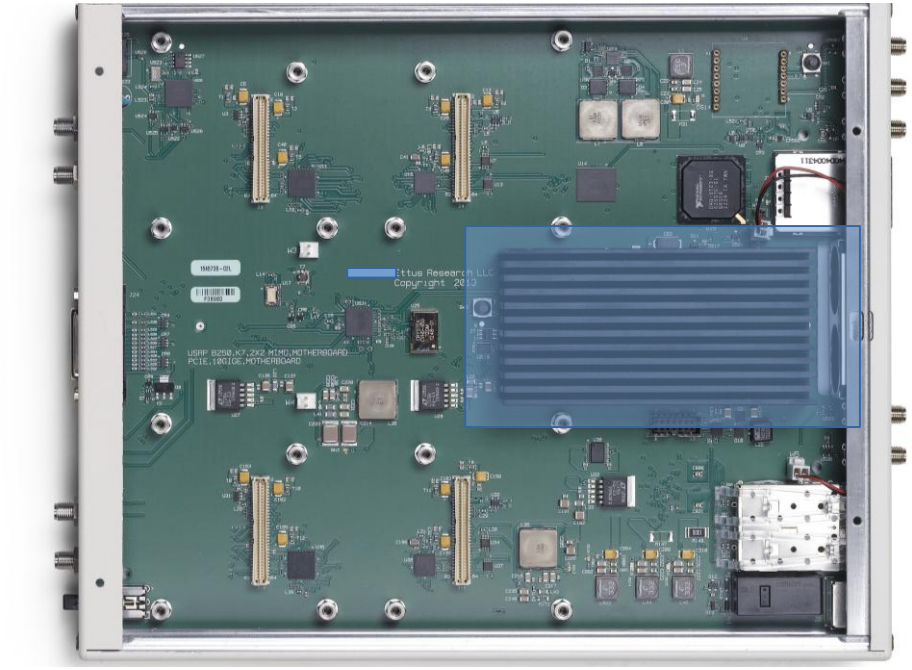
- Everything USRP is available online (code, schematics)
- Contains big and expensive FPGA!



FPGAs: Hard to use… slow to develop

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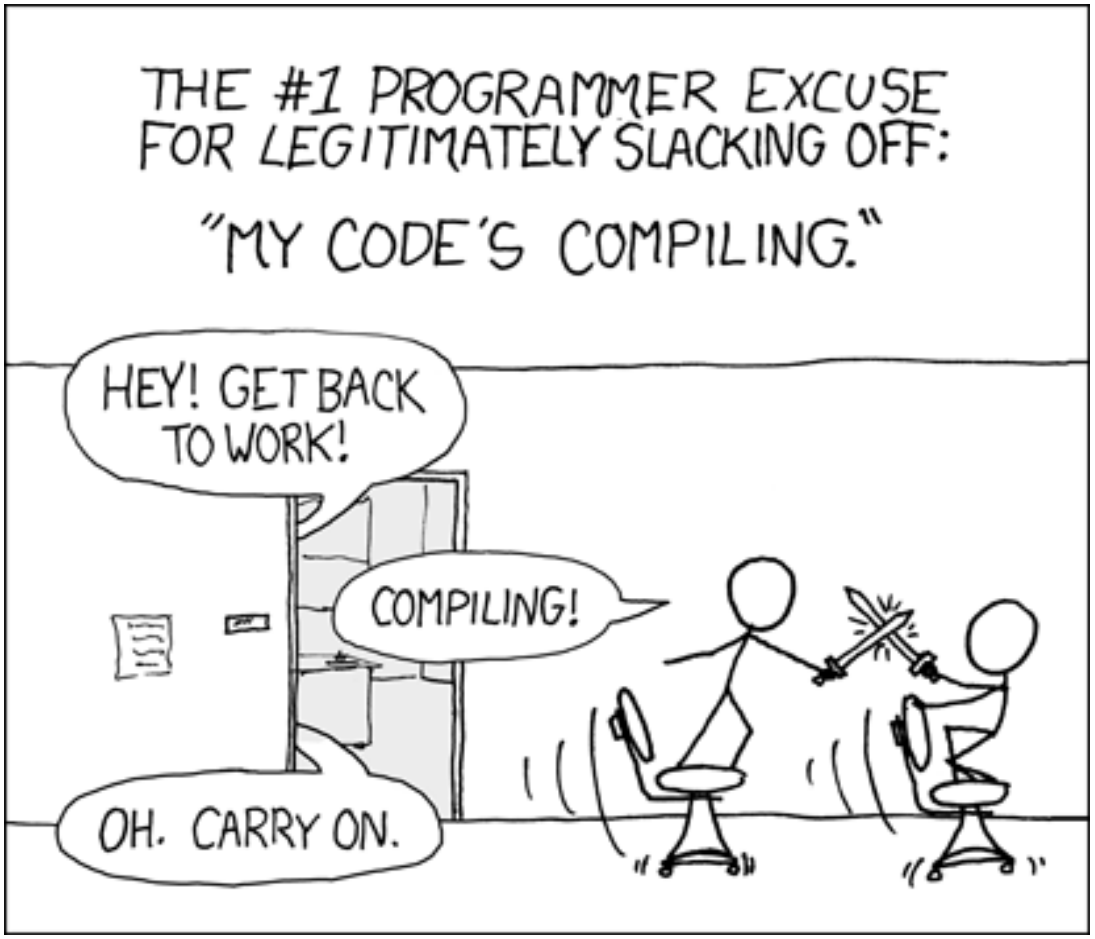

Domain vs FPGA Experts

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- Know Thy Audience!
- FPGA development is not a requirement of a communications engineering curriculum
- Math is hard too

almost pure-noise channels. This intuition is clarified more by the following inequality. It is shown in [1] that for any B-DMC W,

$$1 - I(W) \leqslant Z(W) \leqslant \sqrt{1 - I(W)^2} \tag{2}$$

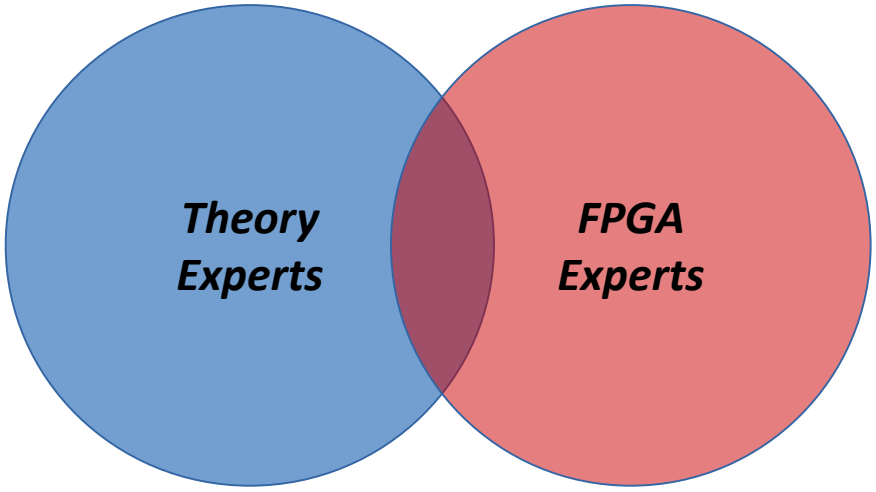
where $I(W)$ is the symmetric capacity of W.

Let W^N denote the channels that results from N independent copies of W i.e. the channel $\langle \{0,1\}^N, \mathscr{Y}^N, W^N \rangle$ given by

$$W^N(y_1^N|x_1^N) \stackrel{\text{def}}{=} \prod_{i=1}^{N} W(y_i|x_i) \tag{3}$$

where $x_1^N = (x_1, x_2, \ldots, x_N)$ and $y_1^N = (y_1, y_2, \ldots, y_N)$. Then the *combined* channel $\langle \{0,1\}^N, \mathscr{Y}^N, \widetilde{W} \rangle$ is defined with transition probabilities given by

$$\widetilde{W}(y_1^N|u_1^N) \stackrel{\text{def}}{=} W^N(y_1^N | u_1^N G_N) = W^N(y_1^N | u_1^N R_N G^{\otimes n})$$



Example: Wideband Spectral Analysis

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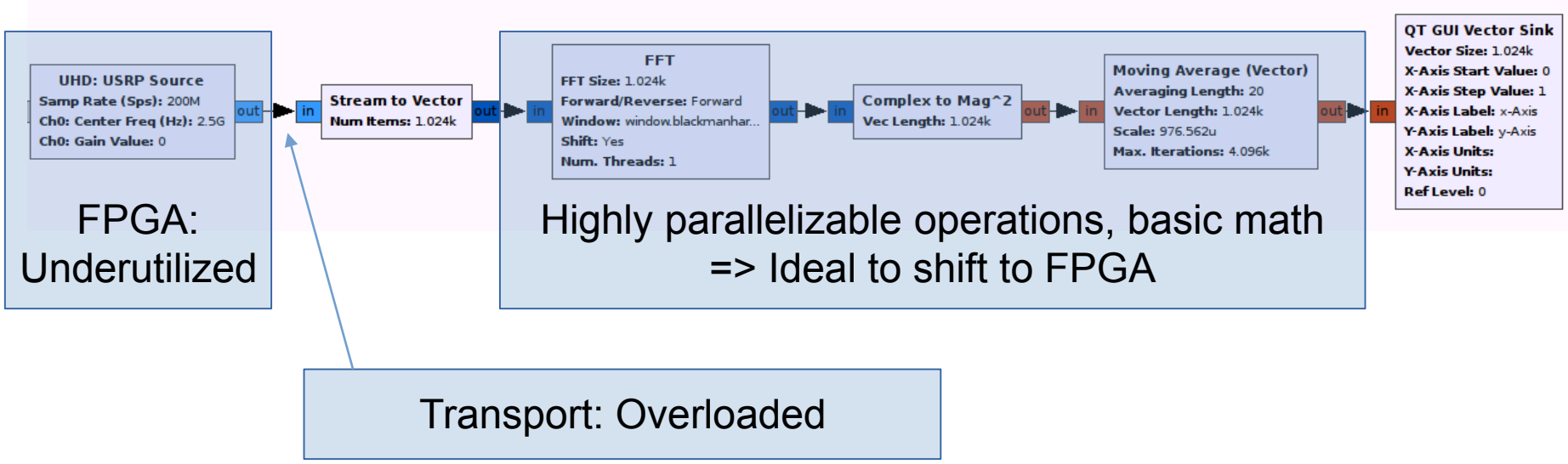
- Simple in Theory: 200 MHz real-time, Welch's Algorithm



Goal

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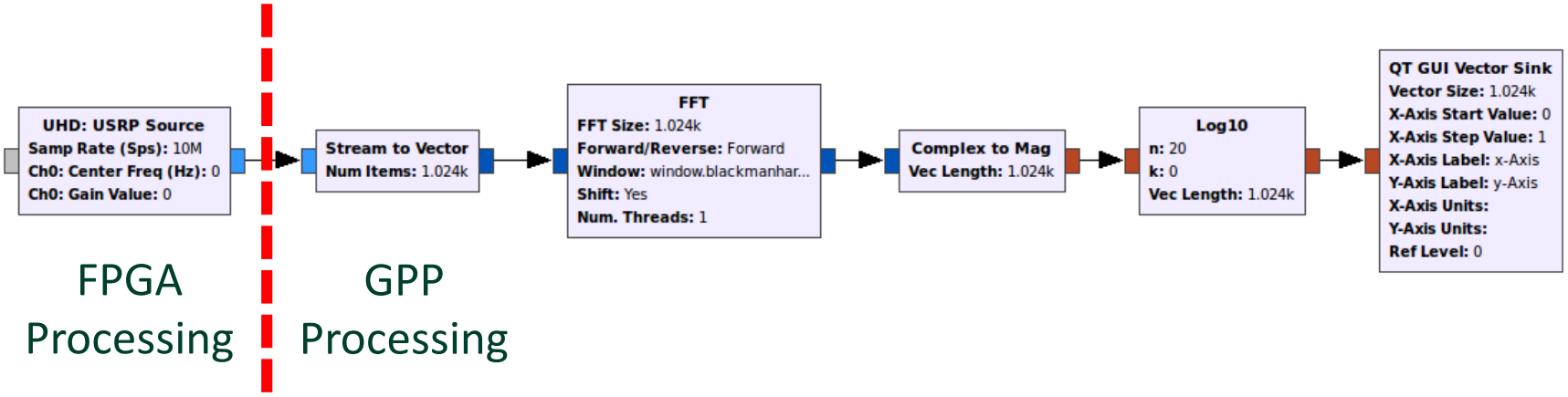
- Heterogeneous Processing
- Support composable and modular designs using GPP, FPGA, & beyond
- Maintain ease of use
- Tight integration with popular SDR frameworks



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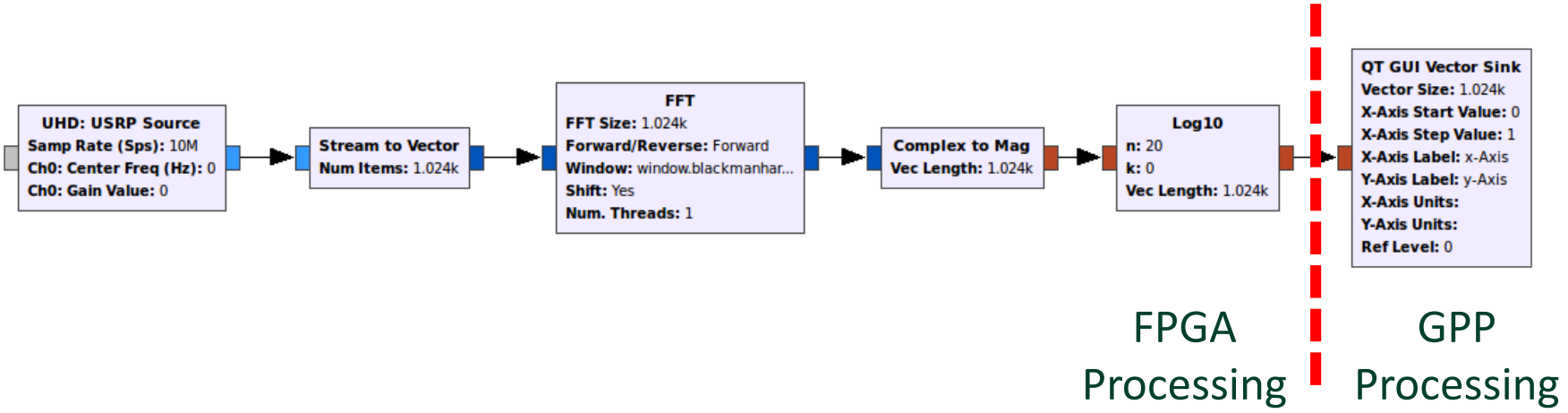

RFNoC: RF Network on Chip

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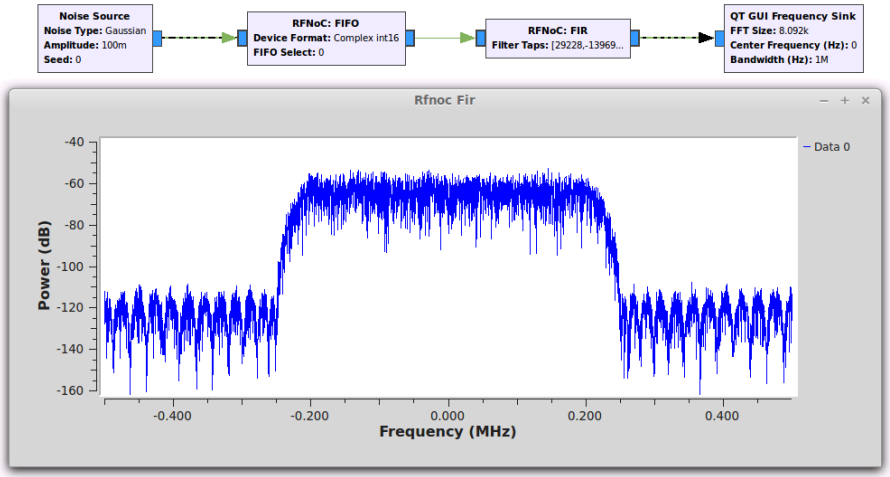
- Make FPGA acceleration easier (especially on USRPs)
  - Software API + FPGA infrastructure
    - Handles FPGA – Host communication / dataflow
    - Provides user simple software and HDL interfaces
  - Scalable design for massive distributed processing
  - Fully supported in GNU Radio



RFNoC Architecture

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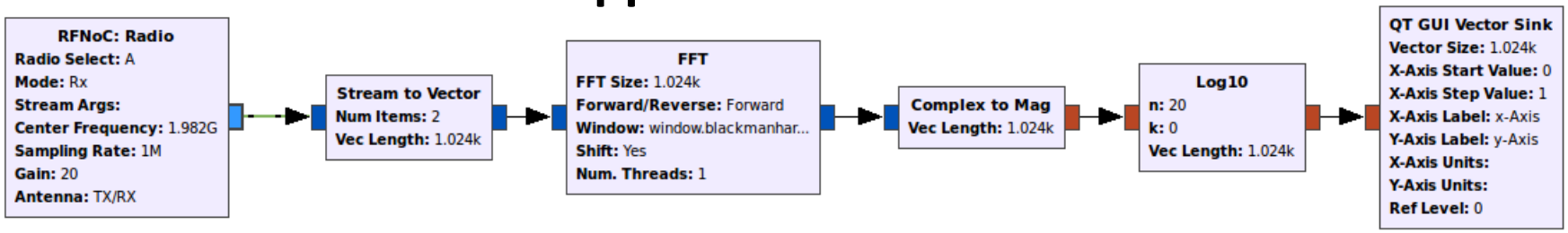
User Application – GNU Radio



HOST PC

USRP Hardware Driver

Ingress Egress Interface

Crossbar

USRP FPGA

Radio Core

Computation Engine

Computation Engine

RFNoC Architecture

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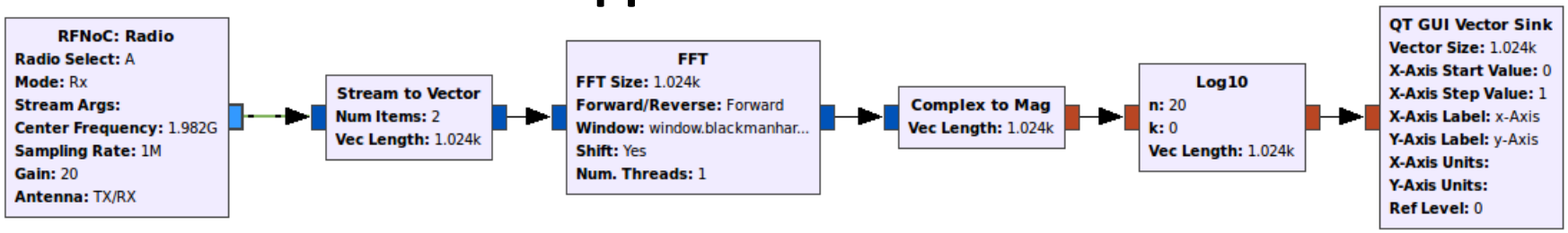
User Application – GNU Radio



- Example: Plotting frequency spectrum

HOST PC

Ingress Egress Interface

Crossbar

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USRP FPGA

RFNoC Architecture

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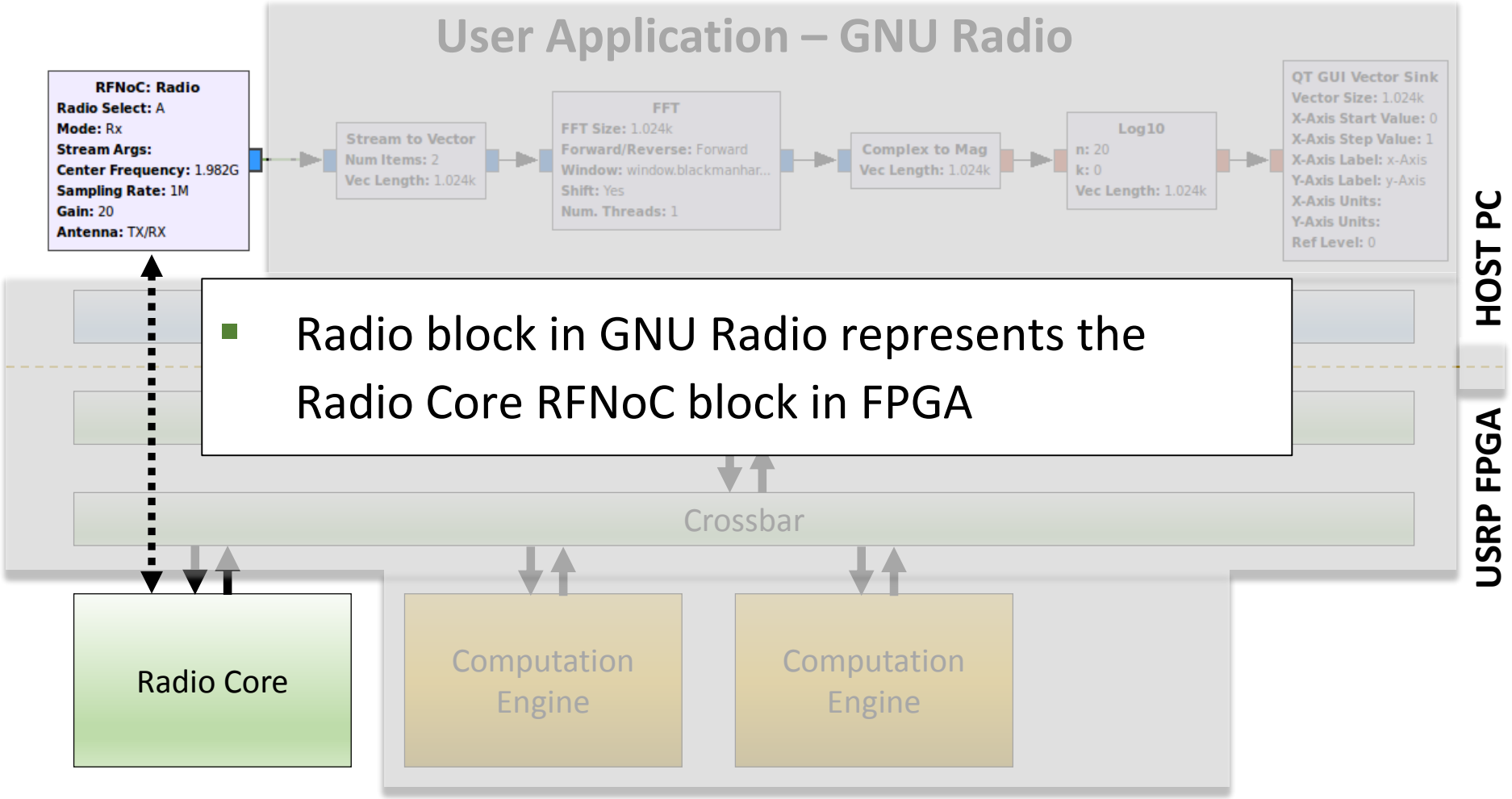

- Radio block in GNU Radio represents the Radio Core RFNoC block in FPGA

RFNoC Architecture

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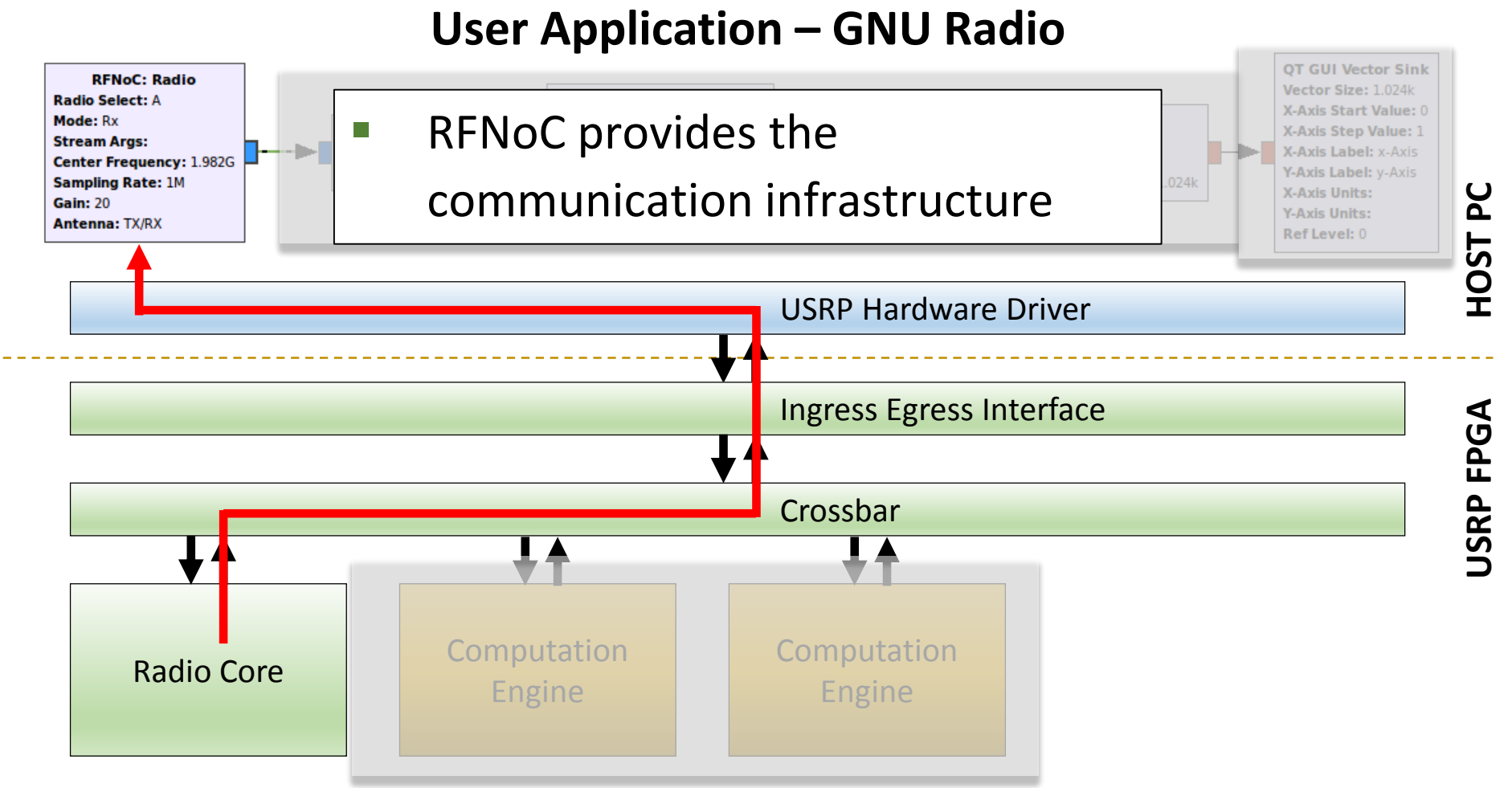

RFNoC Architecture

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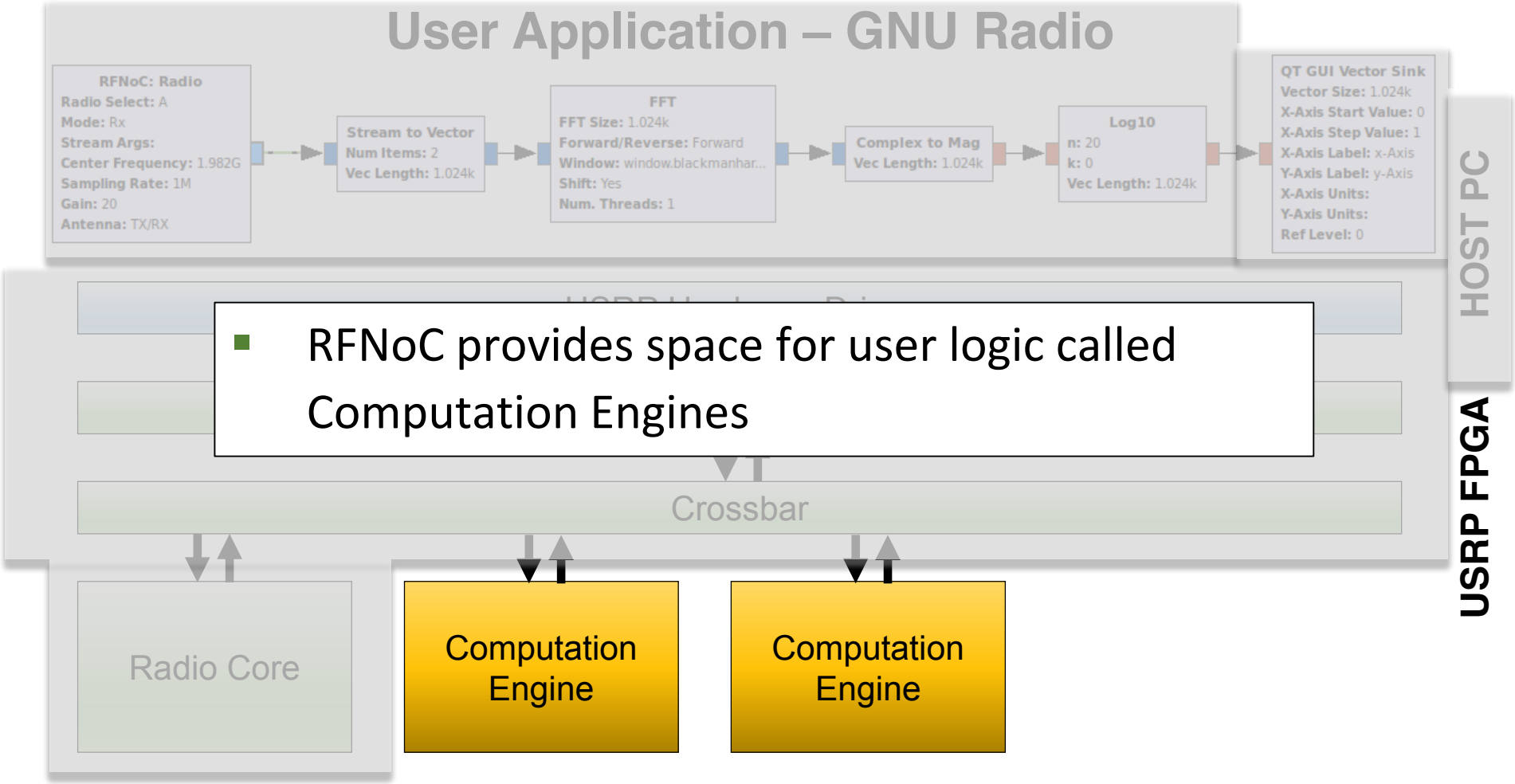

RFNoC Architecture

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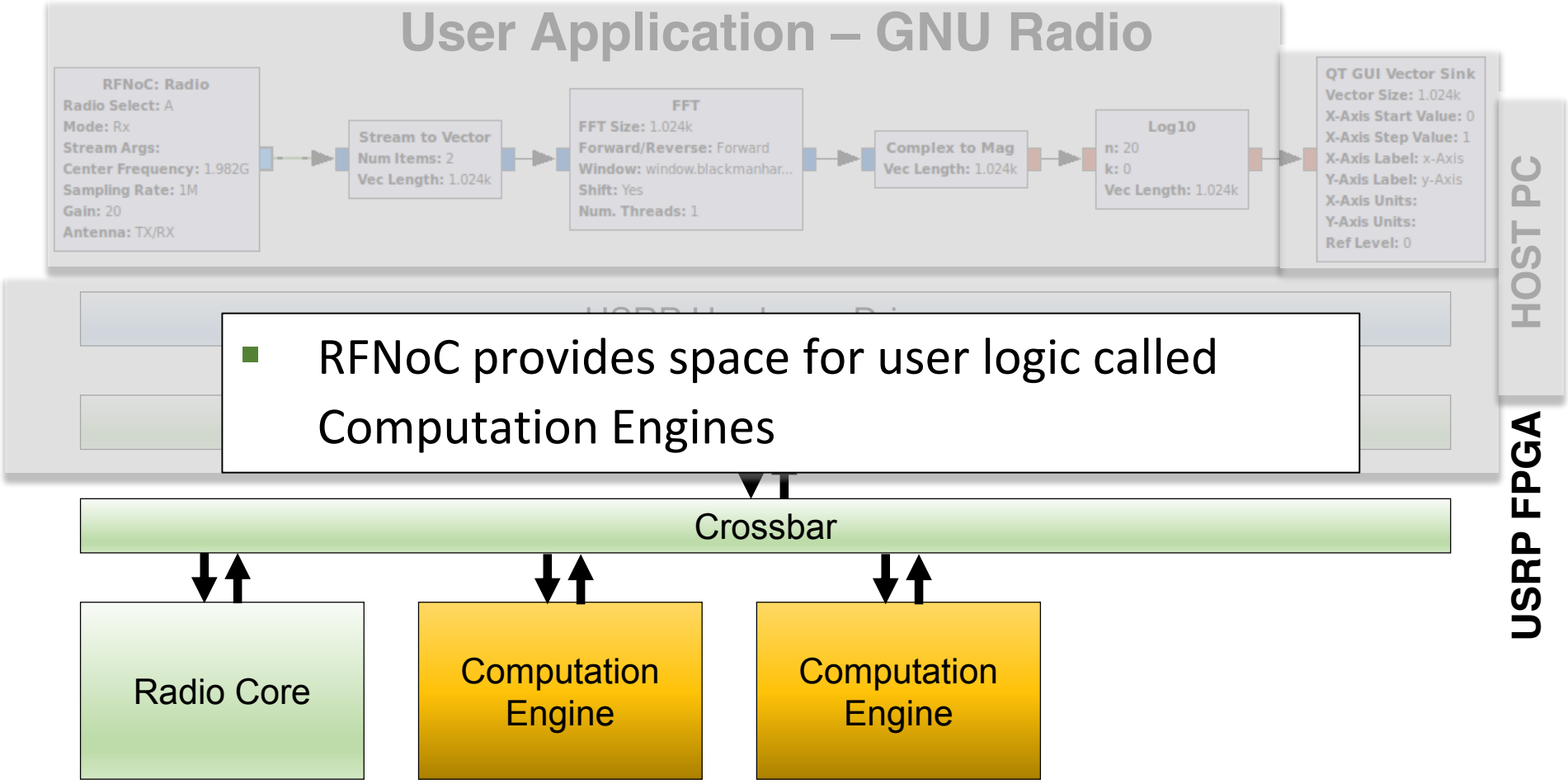

RFNoC Architecture

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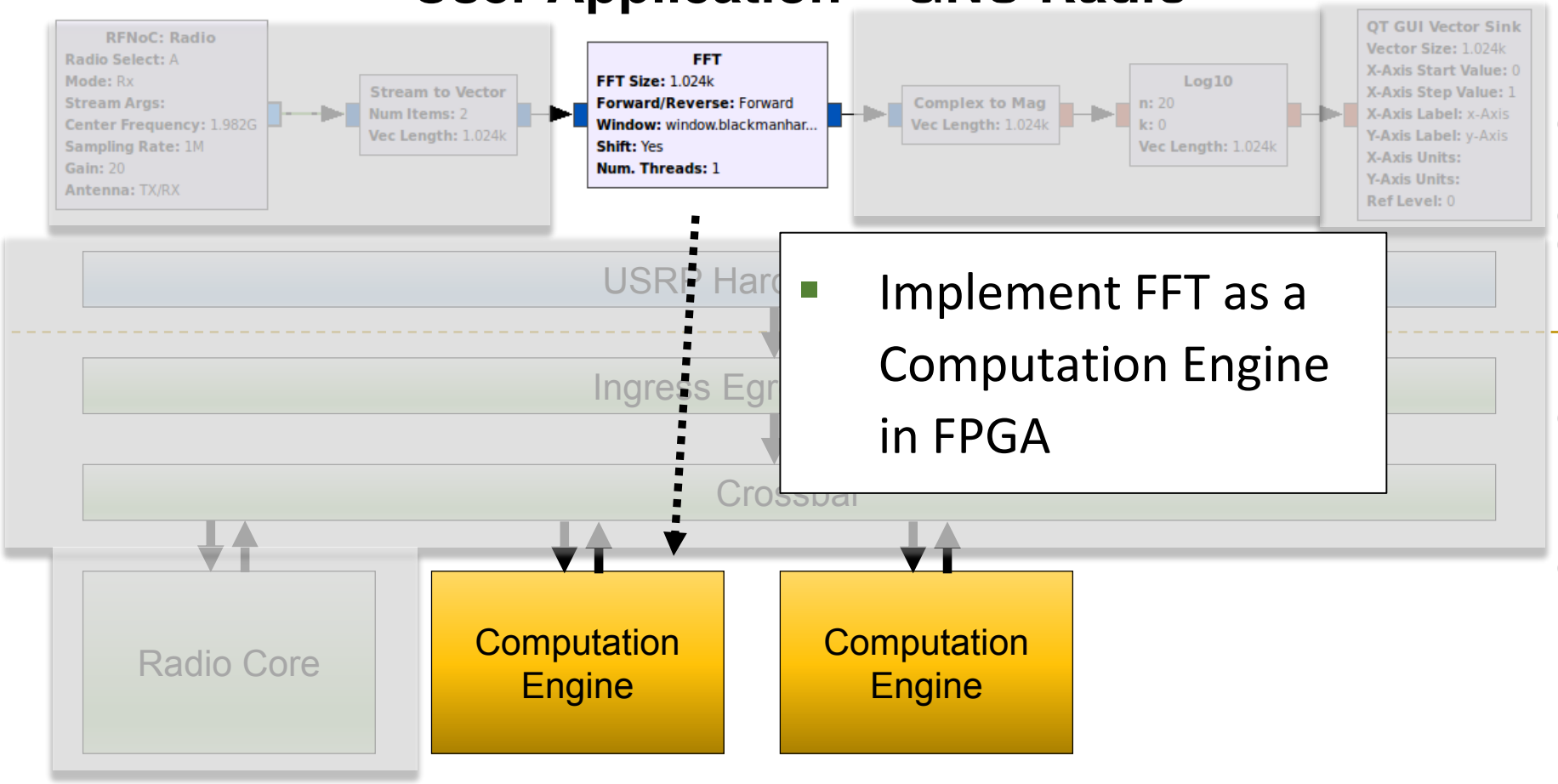
User Application – GNU Radio



- Implement FFT as a Computation Engine in FPGA

RFNoC Architecture

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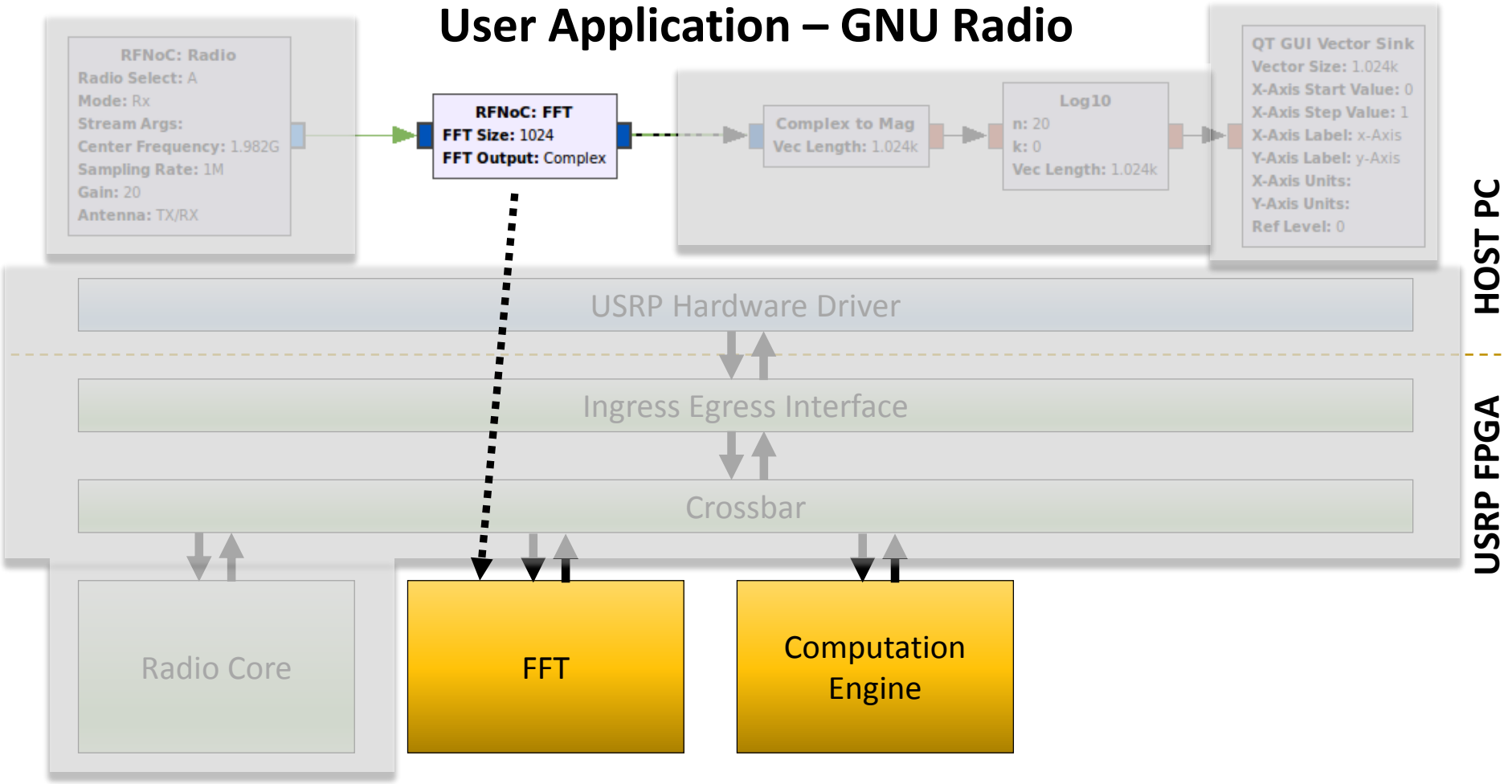

RFNoC Architecture

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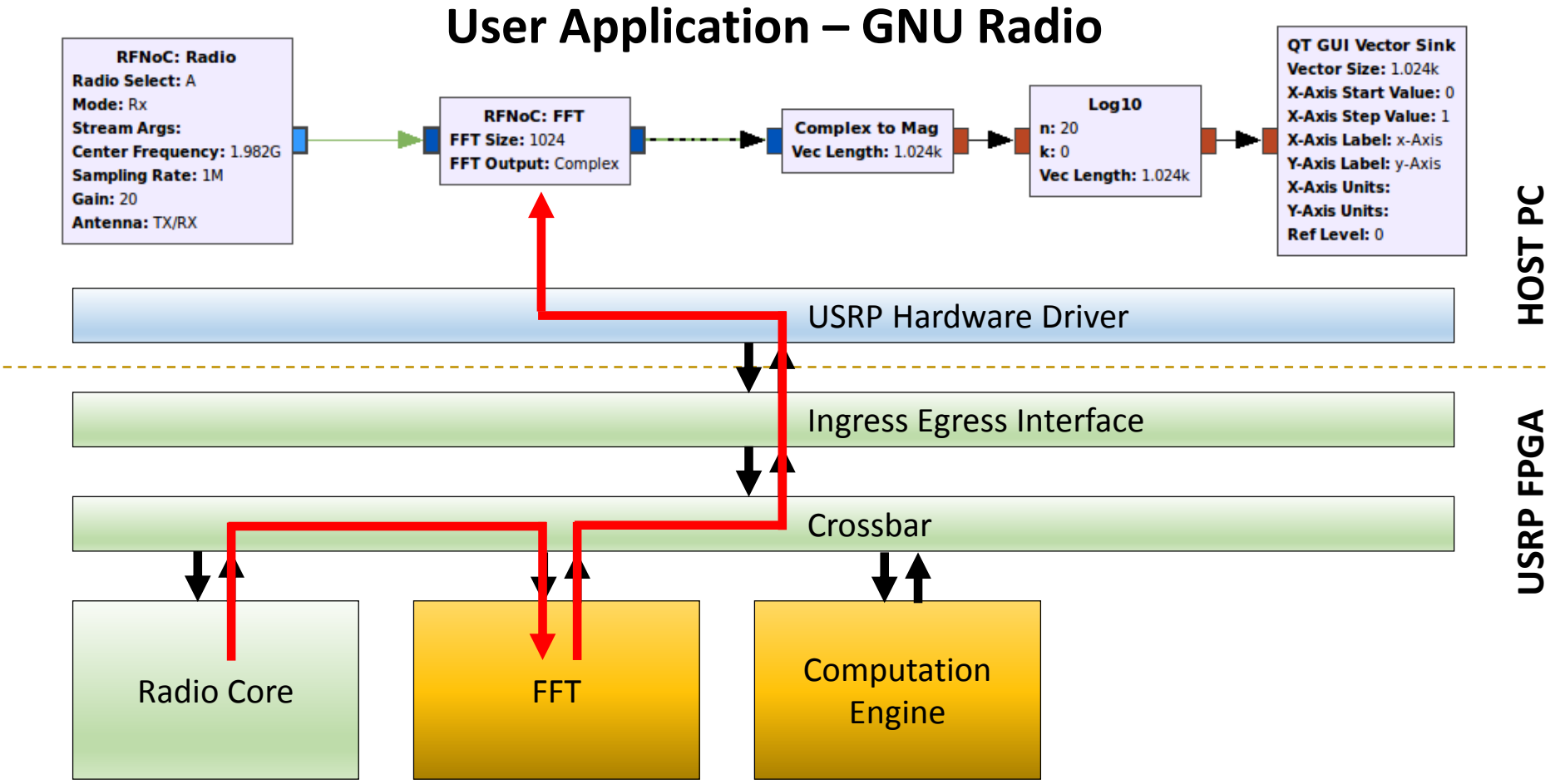

Computation Engine

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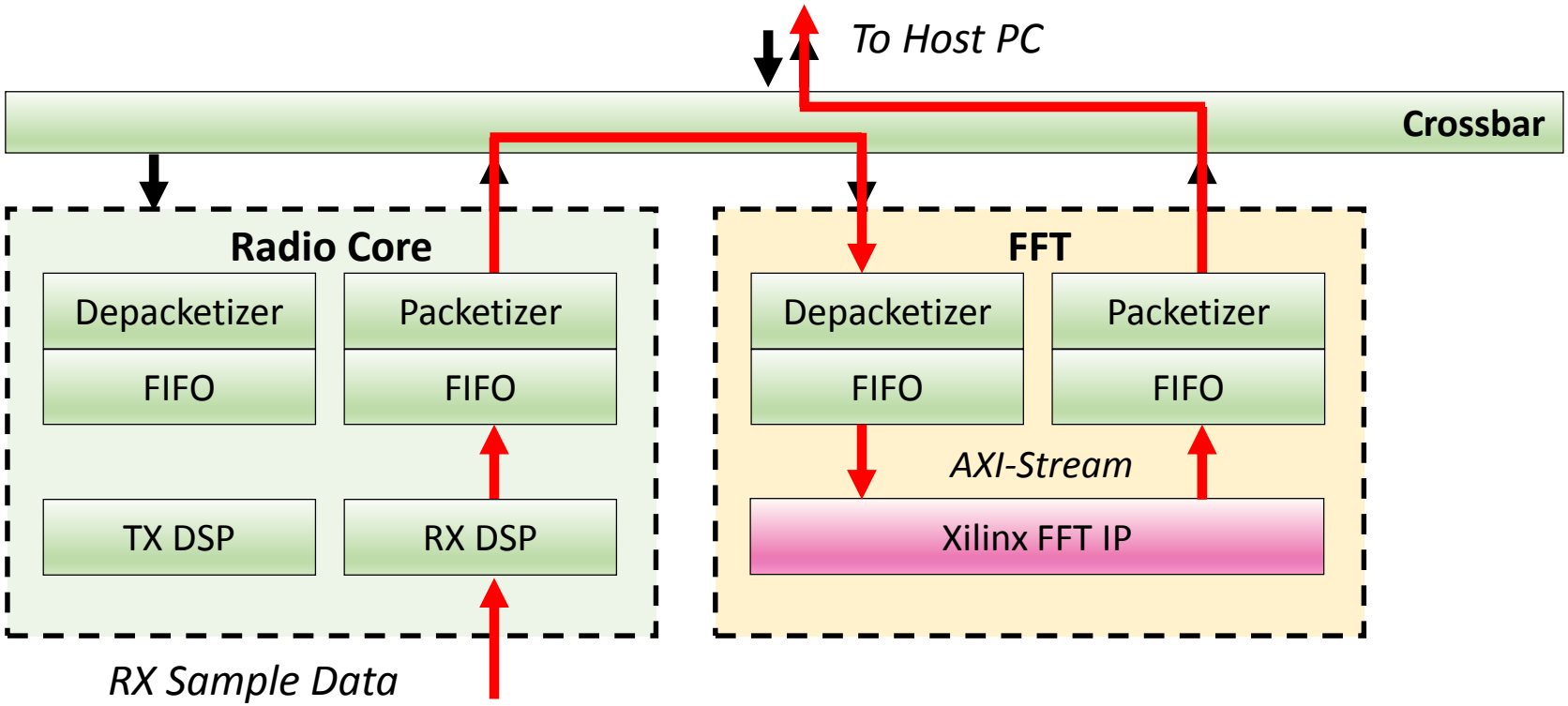
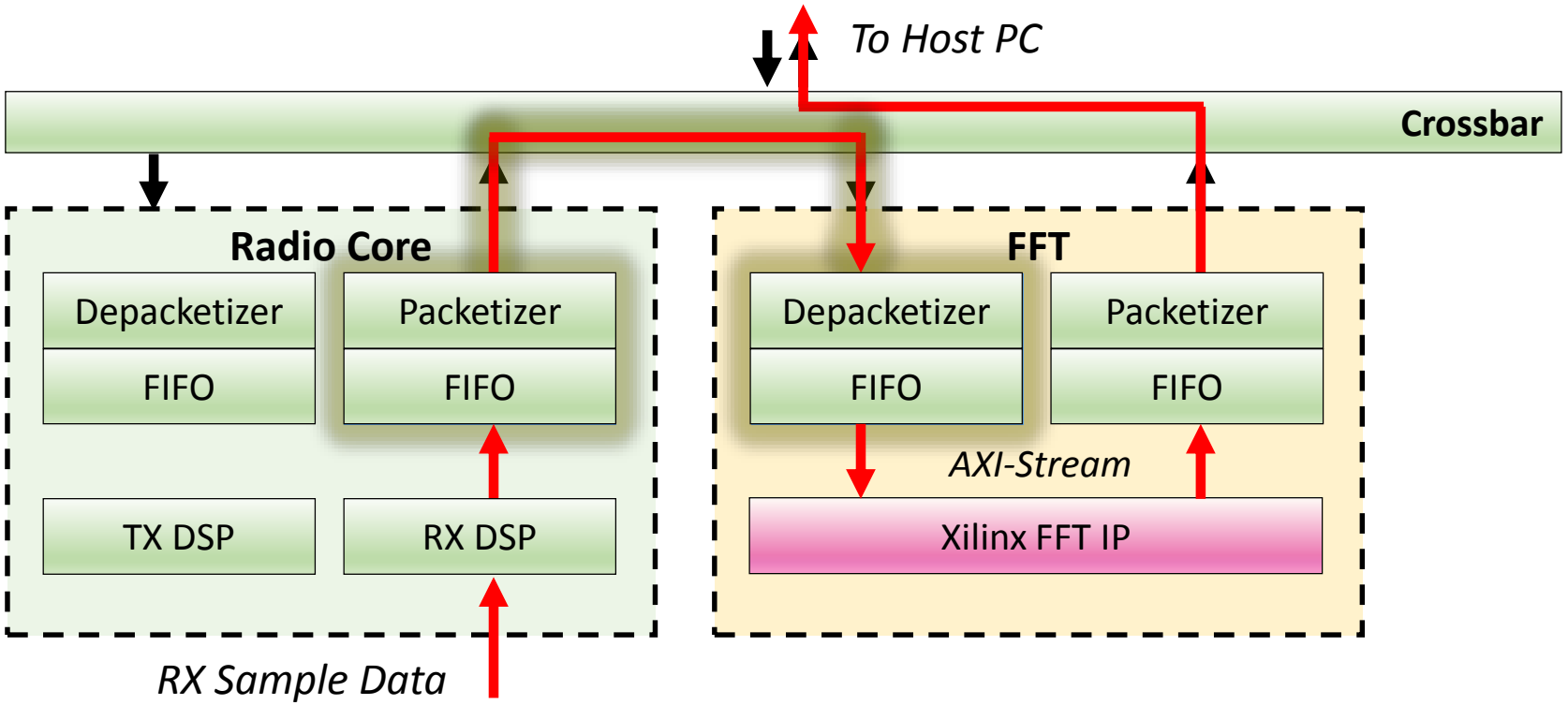


Computation Engine



- FIFO to FIFO, packetization, flow control
- Provided by RFNoC infrastructure

Computation Engine

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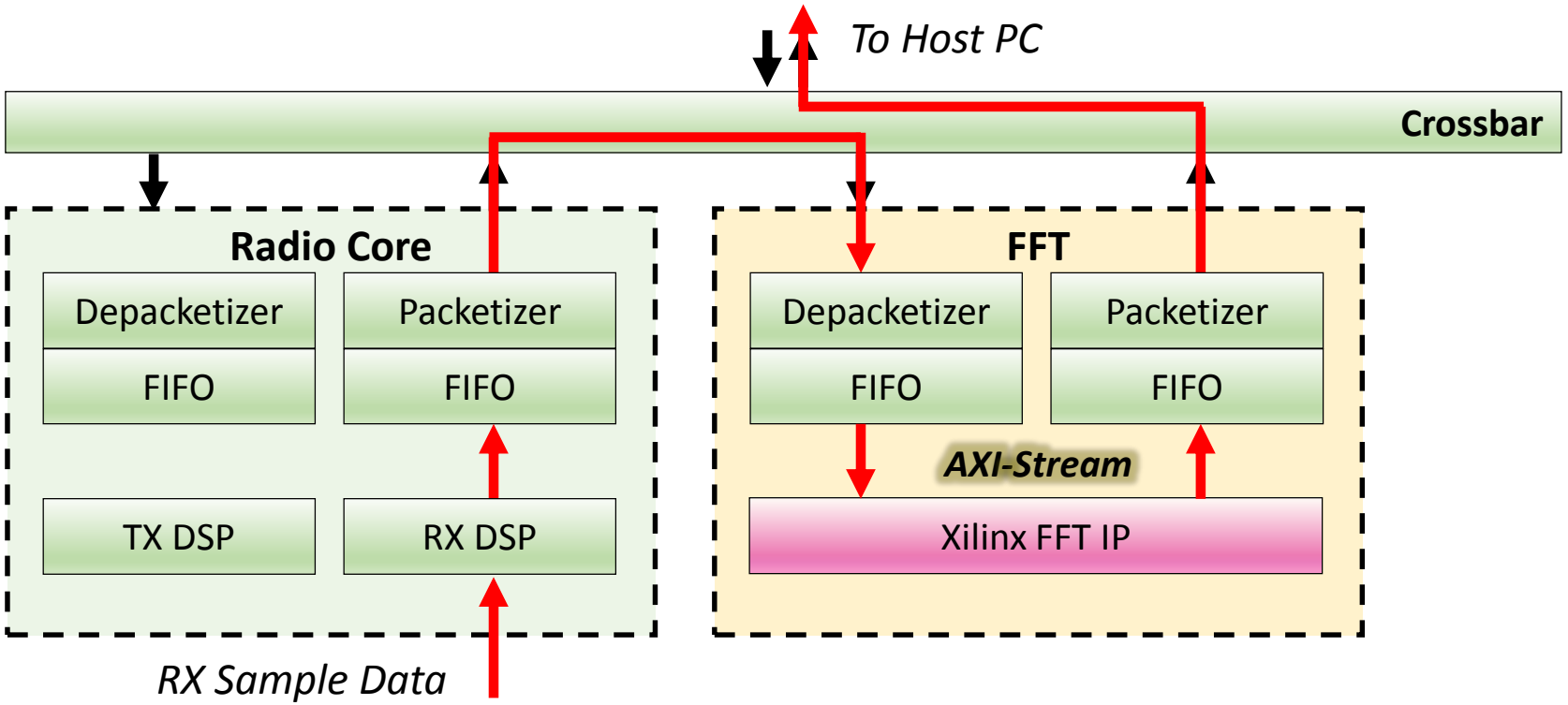
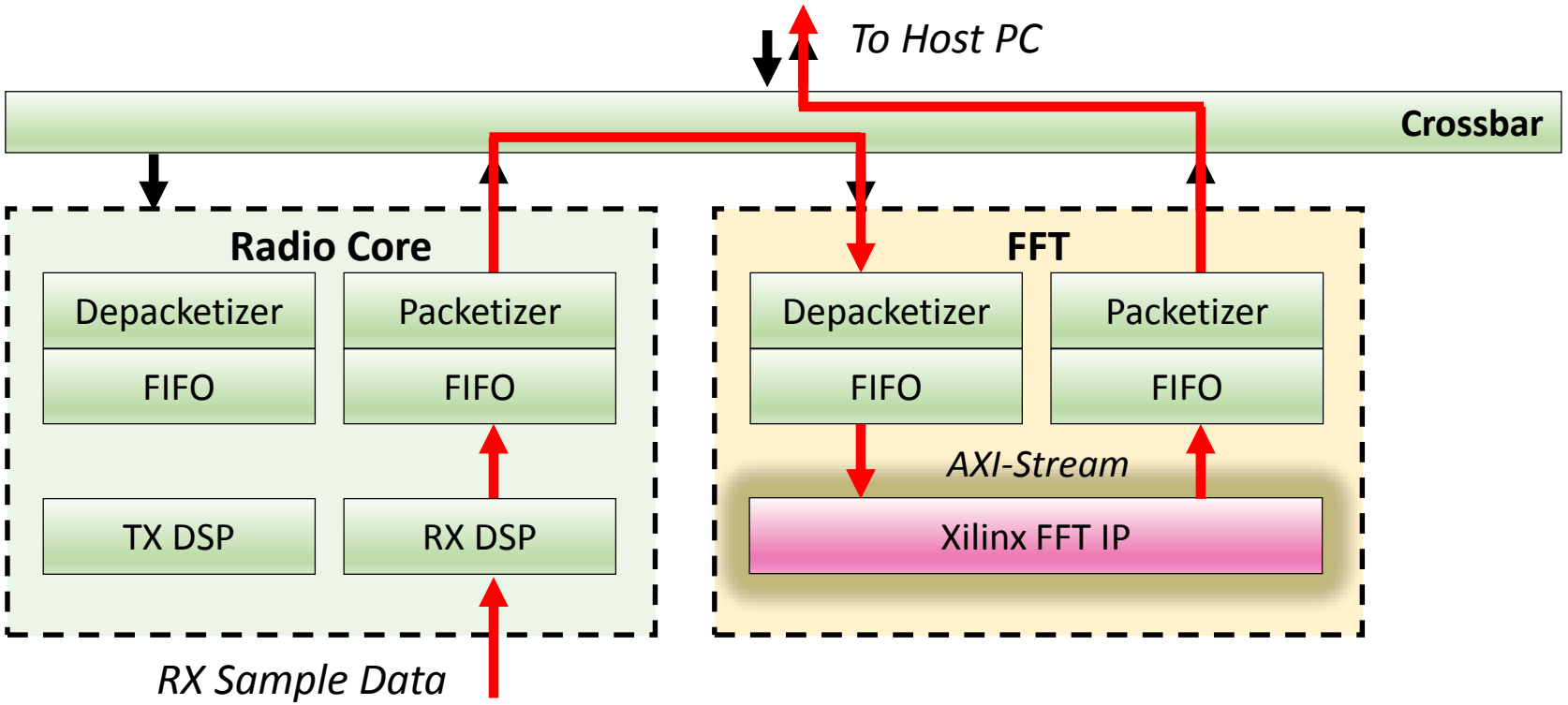


- User interfaces to RFNoC via AXI-Stream
  - Industry standard (ARM), easy to use
  - Large library of existing IP cores

Computation Engine



- User writes their own HDL or drops in IP
  - Multiple AXI-Streams, Control / Status registers

Computation Engine

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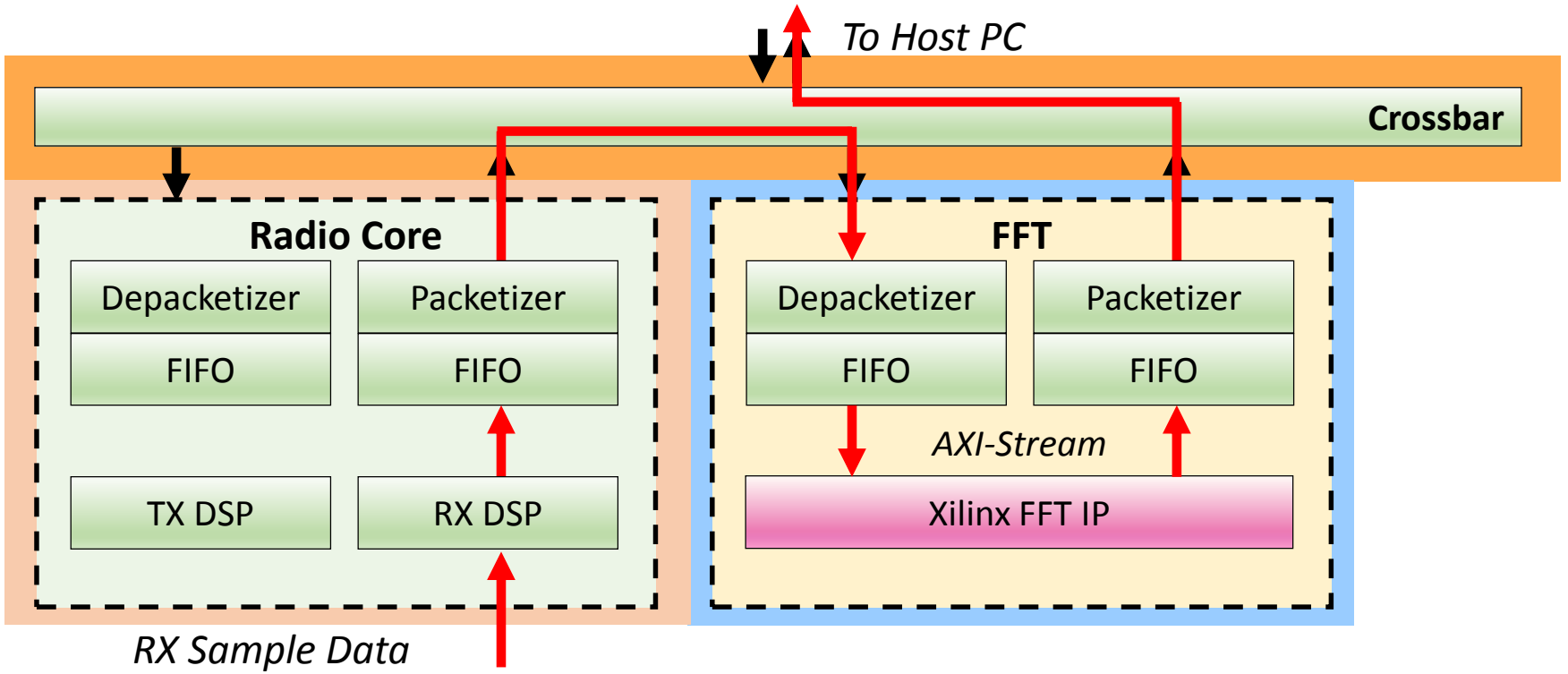
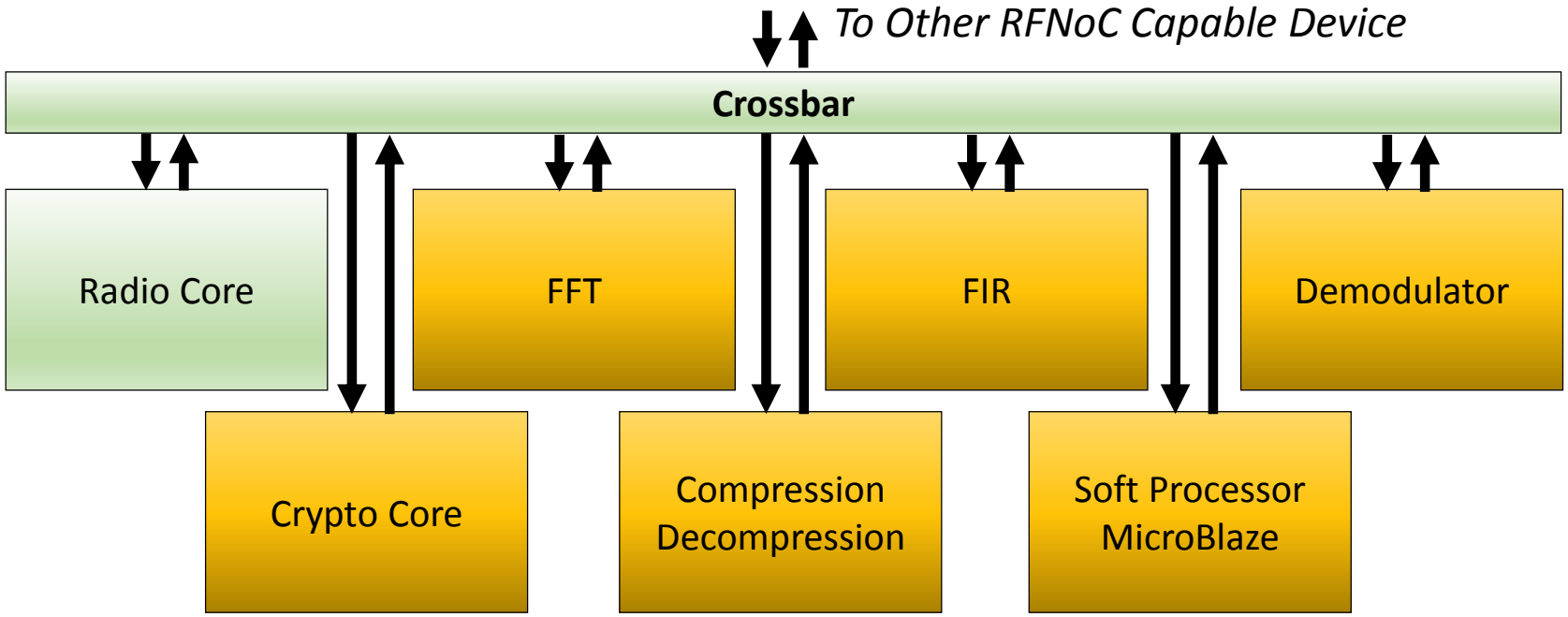


- Each block is in their own clock domain
  - Improve block throughput, timing
  - Interface to Crossbar has clock crossing FIFOs

Many Types of CEs



- Many computation engines
- Not limited to one crossbar, one device
  - Scales across devices for massive distributed processing

Many Types of CEs

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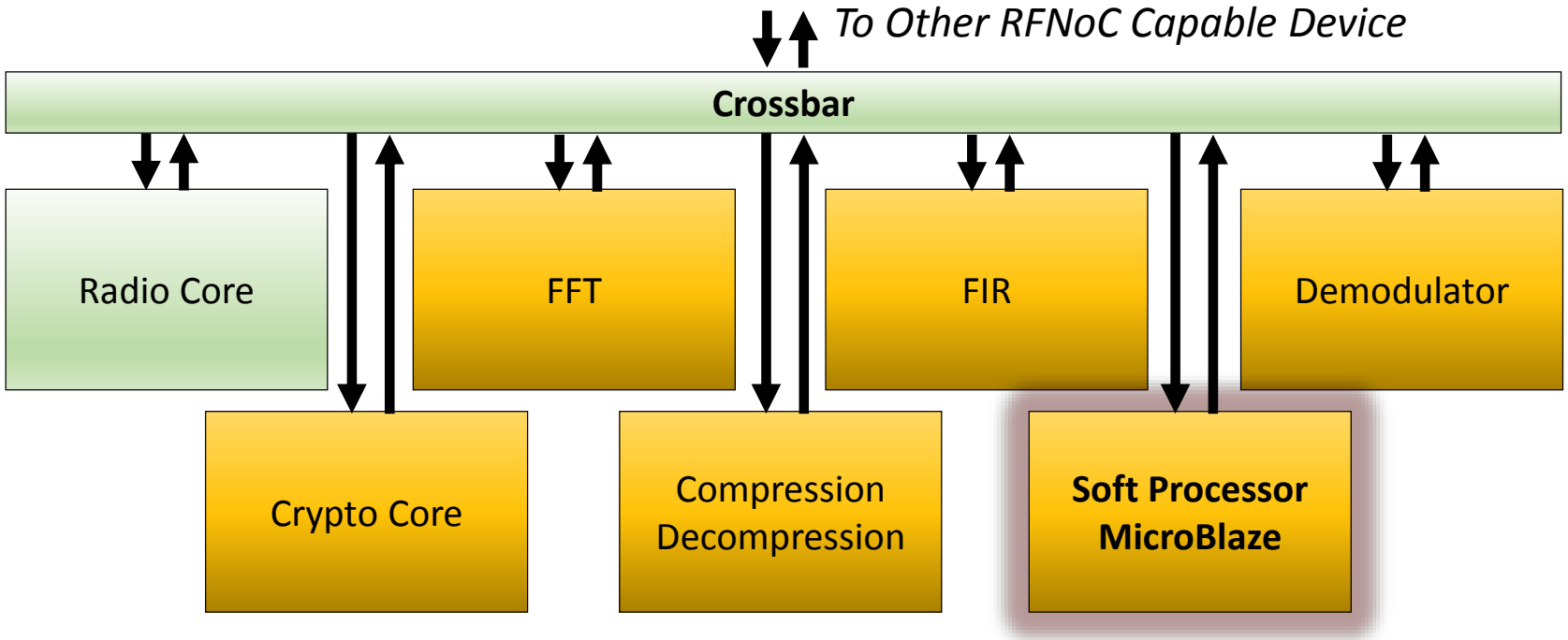

- Low latency protocol processing in FPGA

RFNoC Architecture

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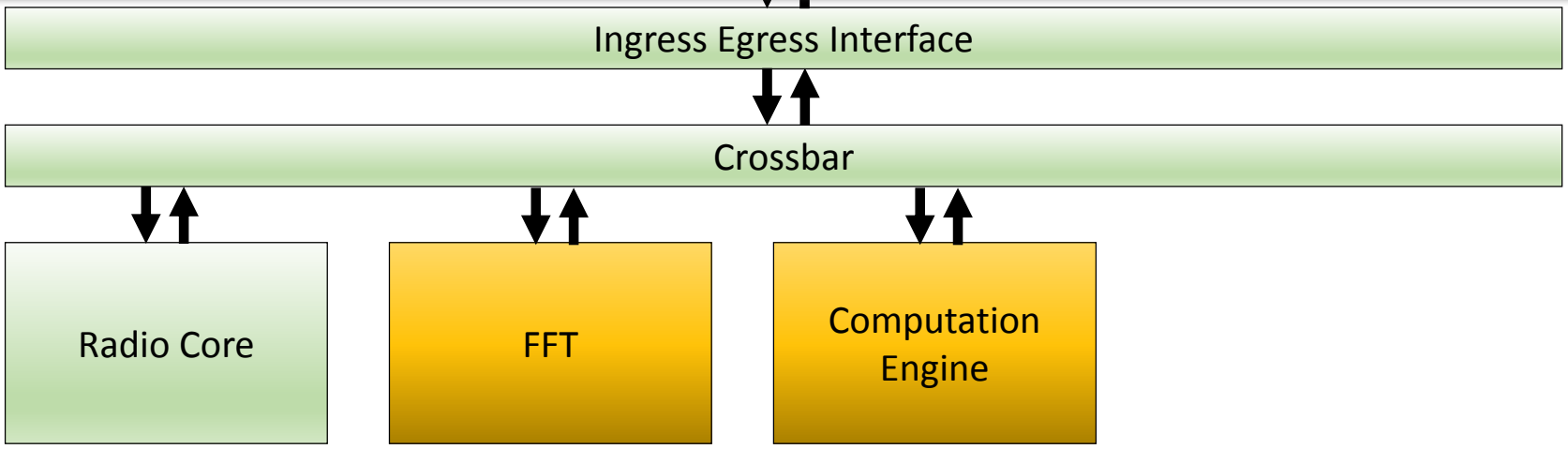
- Transparent protocol conversion
- Multiple standards PCI-E, 10 GigE, AXI
  - Could be wire through -- forwarding to another crossbar
- Parallel interfaces (example: X300 has 2 x 10 GigE)



RFNoC Architecture

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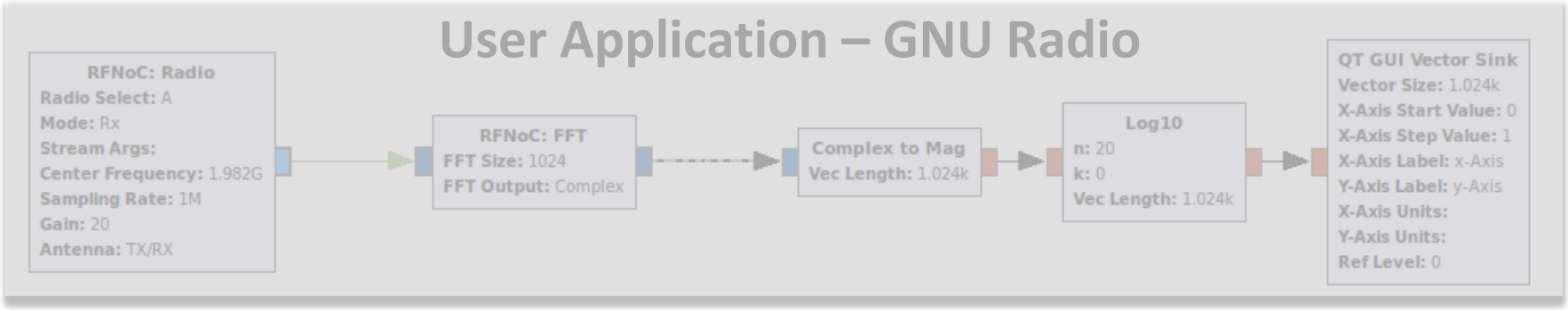

HOST PC

USRP Hardware Driver

USRP FPGA

- Software API to:
  - Configure USRP hardware & RFNoC FPGA infrastructure
  - Provide user sample data (r/w buffers) & control (r/w regs) interfaces

Radio Core

FFT

Computation Engine

RFNoC Architecture

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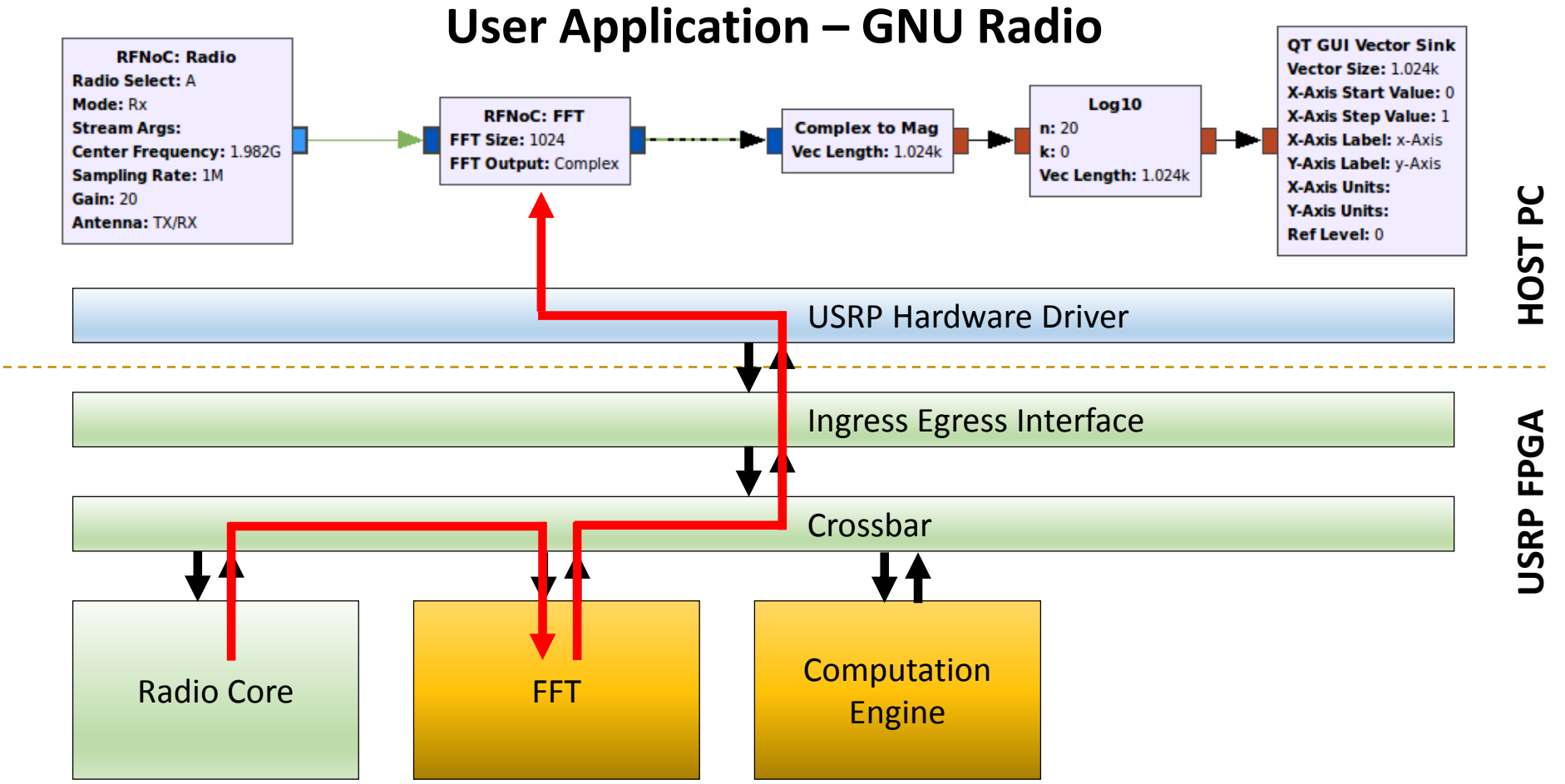

DEMO

Summary

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- Simple architecture for heterogeneous data flow processing
- Implemented several interesting CEs
- Integrated with high level SDR framework
- Portable between all third generation USRPs
  - X3x0, E310, and products soon to come
- Completely open source
- Beta release available!
  - github.com/EttusResearch/uhd/wiki/RFNoC:-Getting-Started