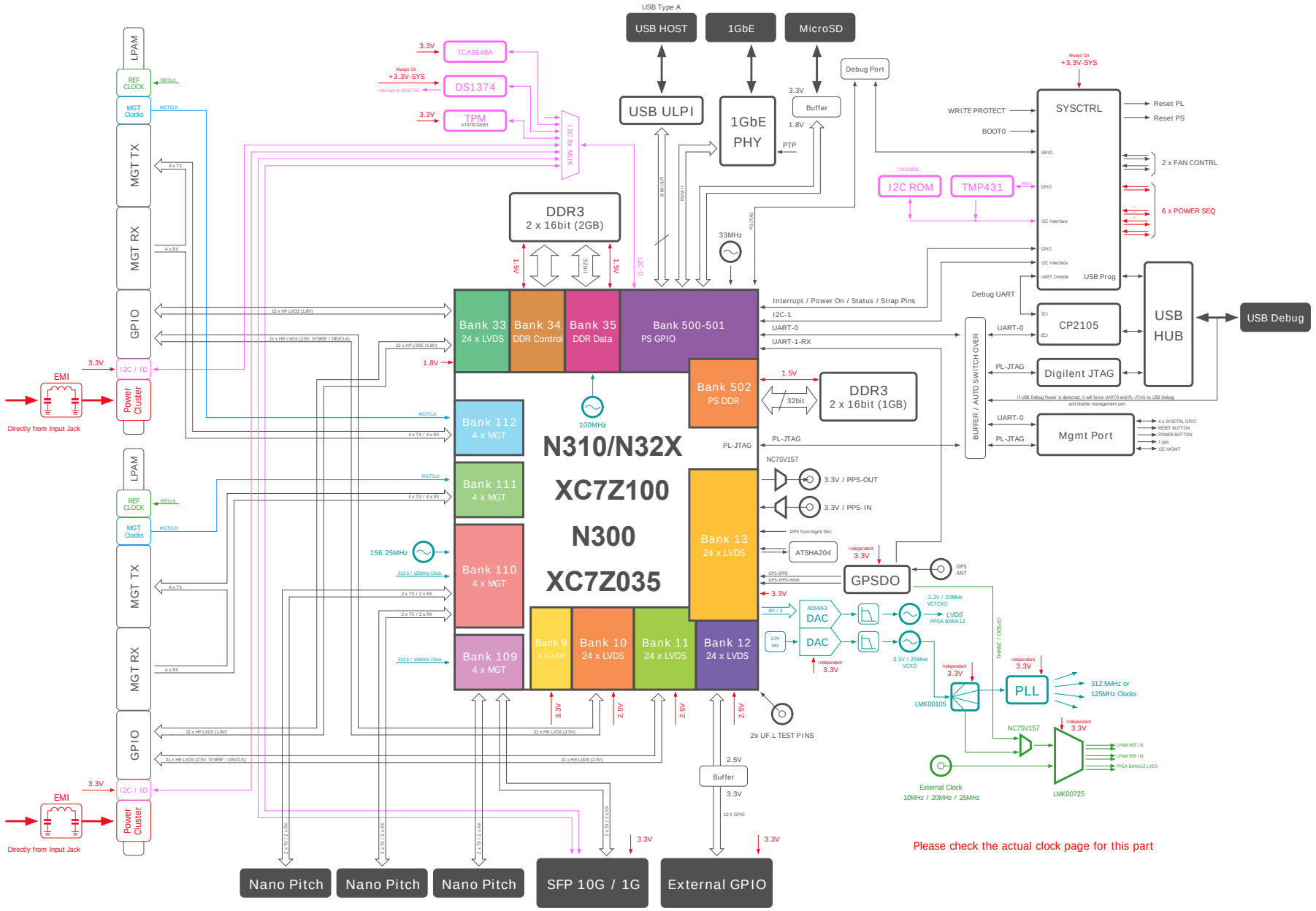

Revisions	
REV	Description

Design Team	
DRAWN BY	DATE
REVISED BY	DATE
VERIFIED BY	
TECHNICIAN	
ENGINEER	

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4600 Patrick Henry Drive
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USA

System Block Diagram

SCH, USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD

SIZE	DOC CODE	DRAWING PROJECT NO	REV
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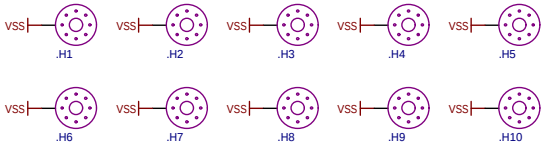
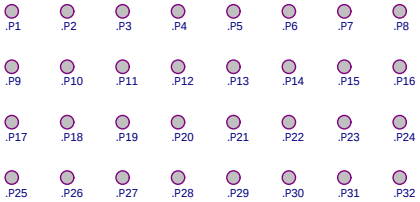
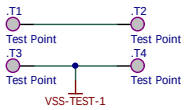
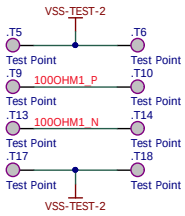
FILE NAME: 01_BlockDiagram.SchDoc | DATE: 5/21/2018 | SHEET 1 OF 25

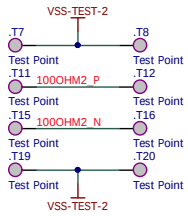
159064F-01

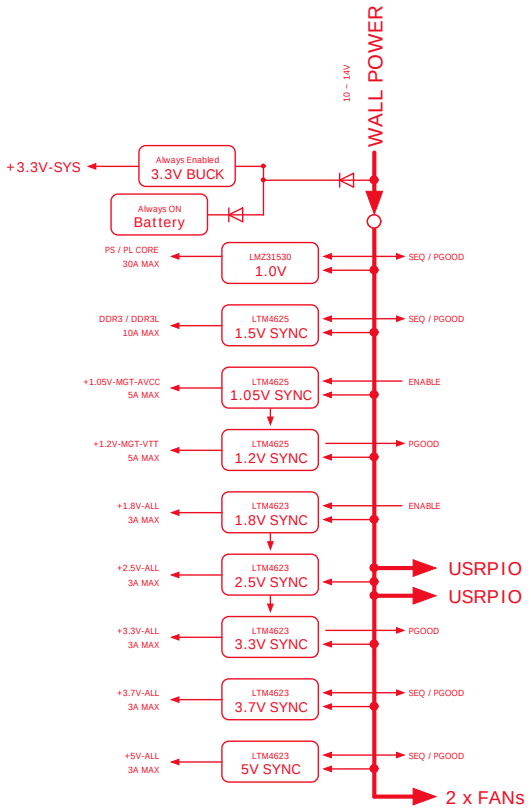












Essential Board Components			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
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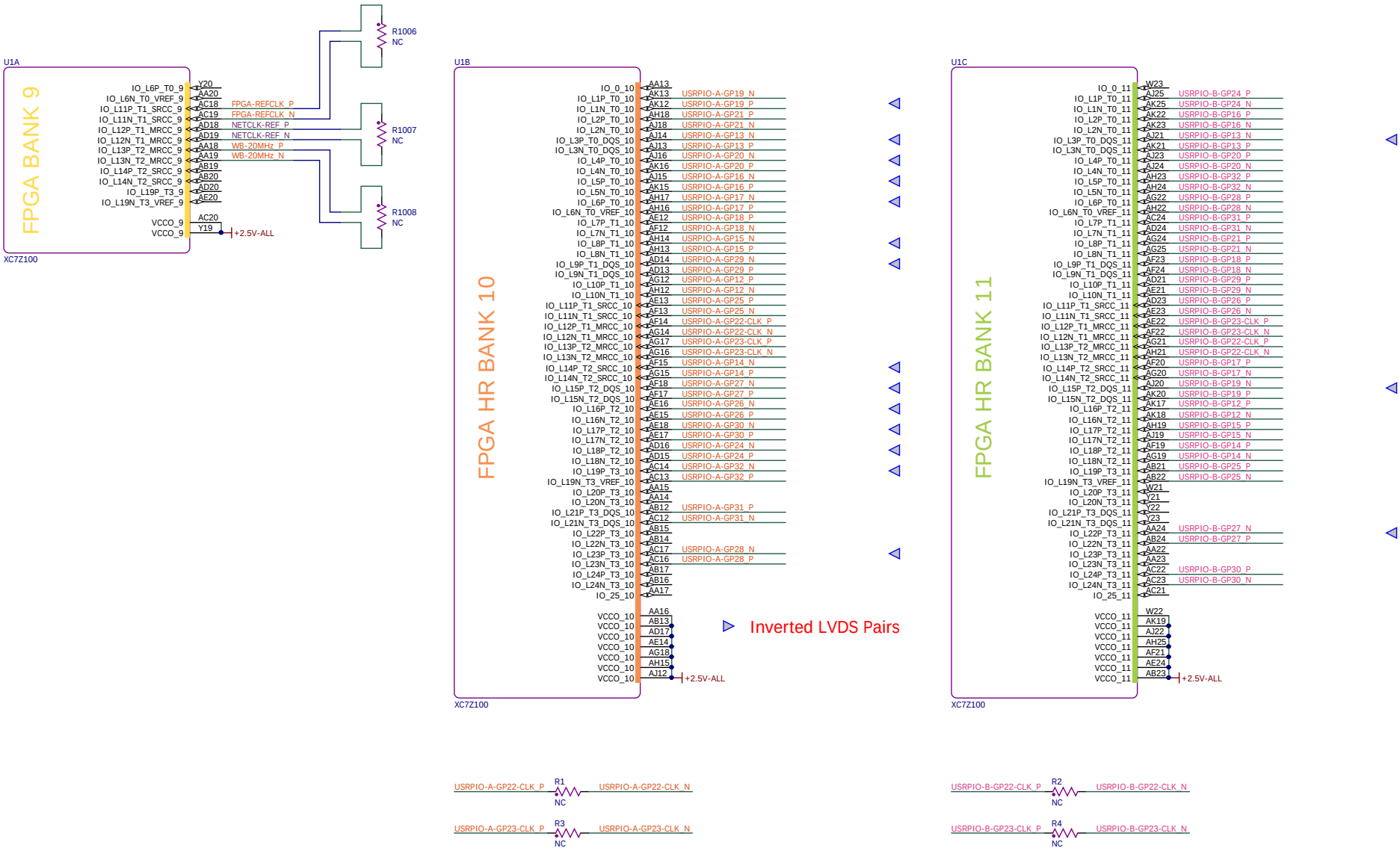
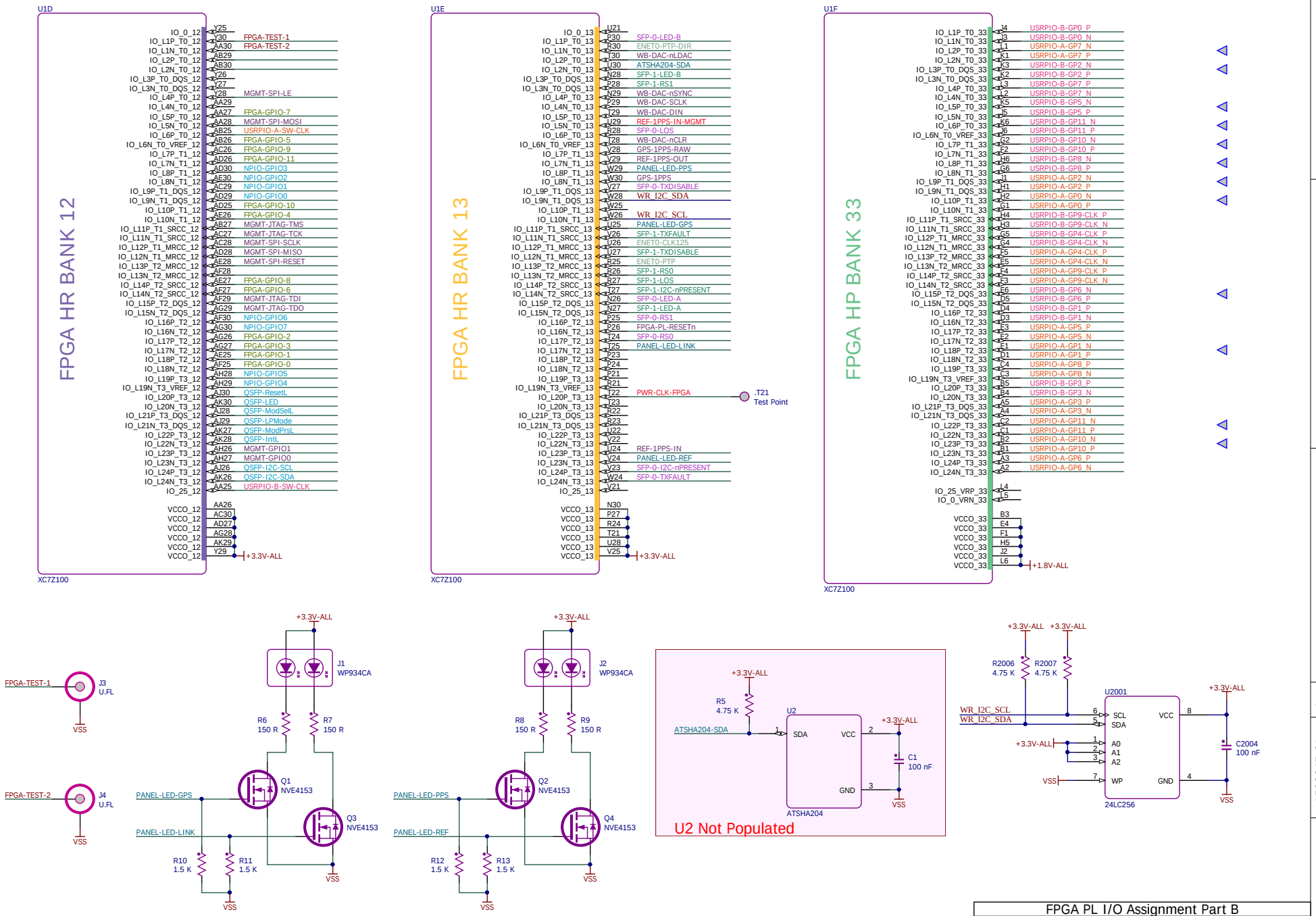
FILE NAME	02_Essential.SchDoc	DATE 5/21/2018	SHEET 2 OF 25

159064F-01



FPGA PL I/O Assignment Part A			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 03_FPGA_PL_IO_A.SchDoc		DATE: 5/21/2018	SHEET 3 OF 25

159064F-01



FPGA PL I/O Assignment Part B			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
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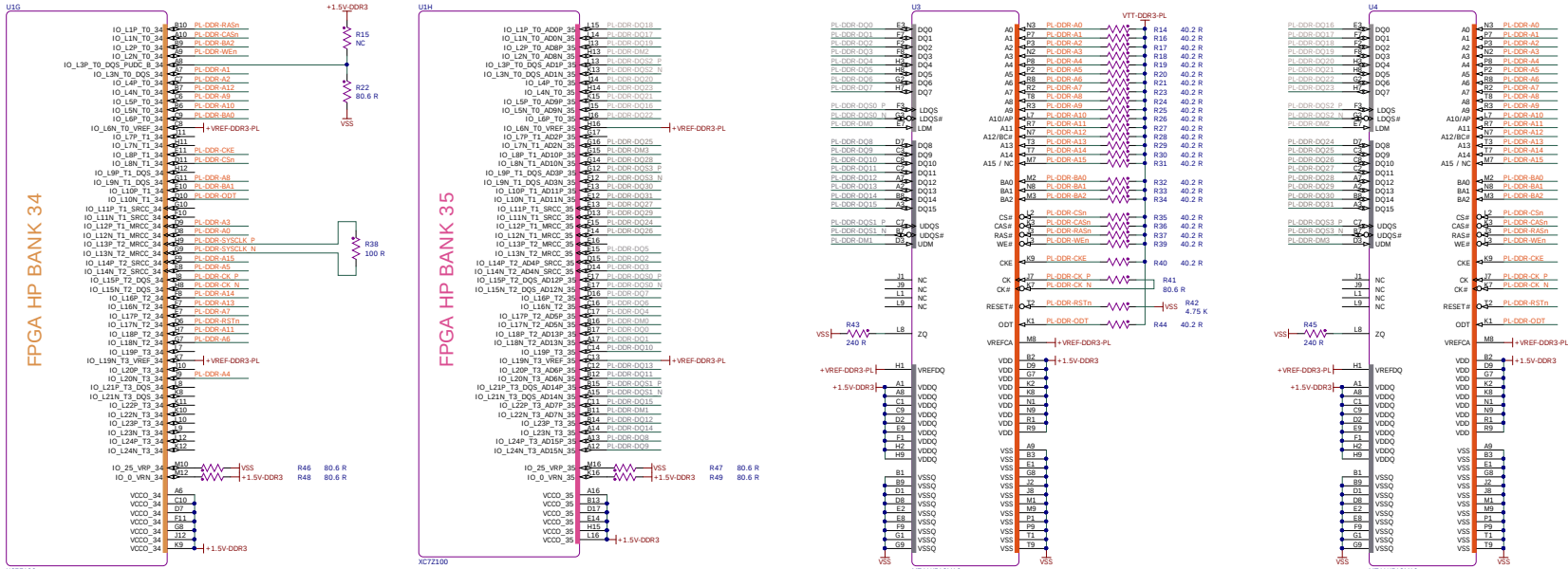

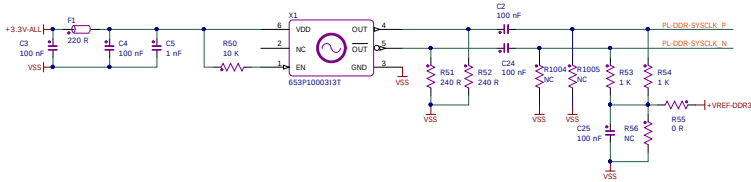

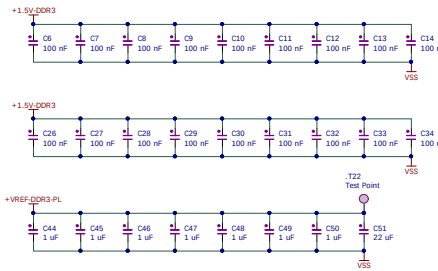

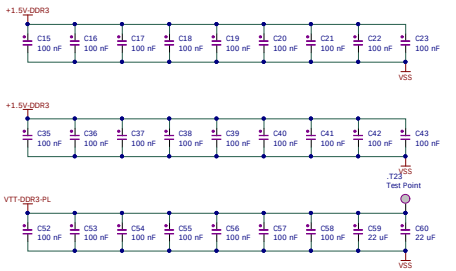

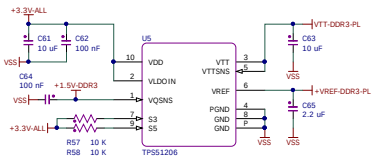

FPGA PL DDR3 Memory			
SCH, USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
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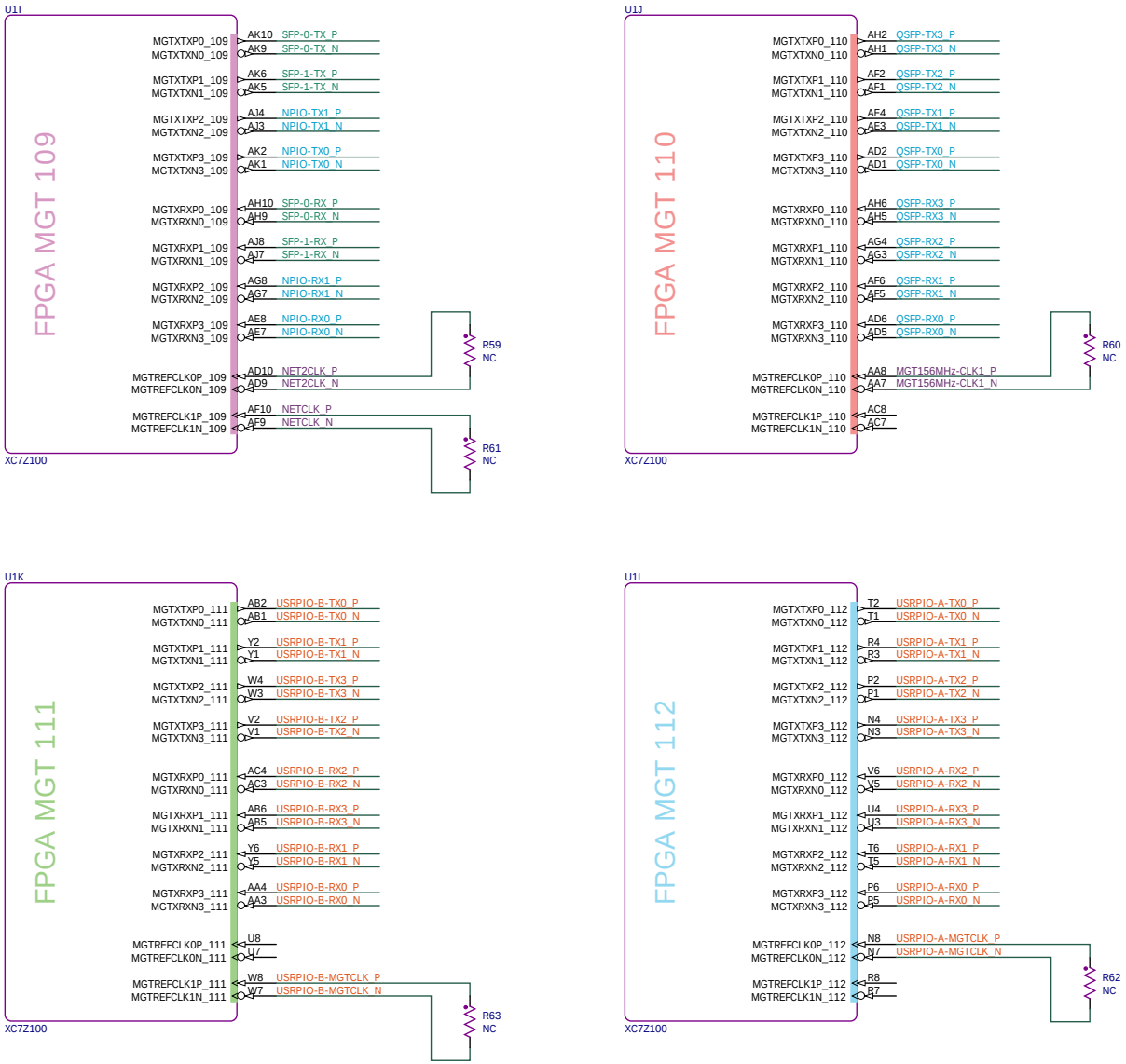
FILE NAME	05_FPGA_PL_DDR.SchDoc	DATE 5/21/2018	SHEET 5 OF 25

159064F-01



FPGA MGT I/O Assignment			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
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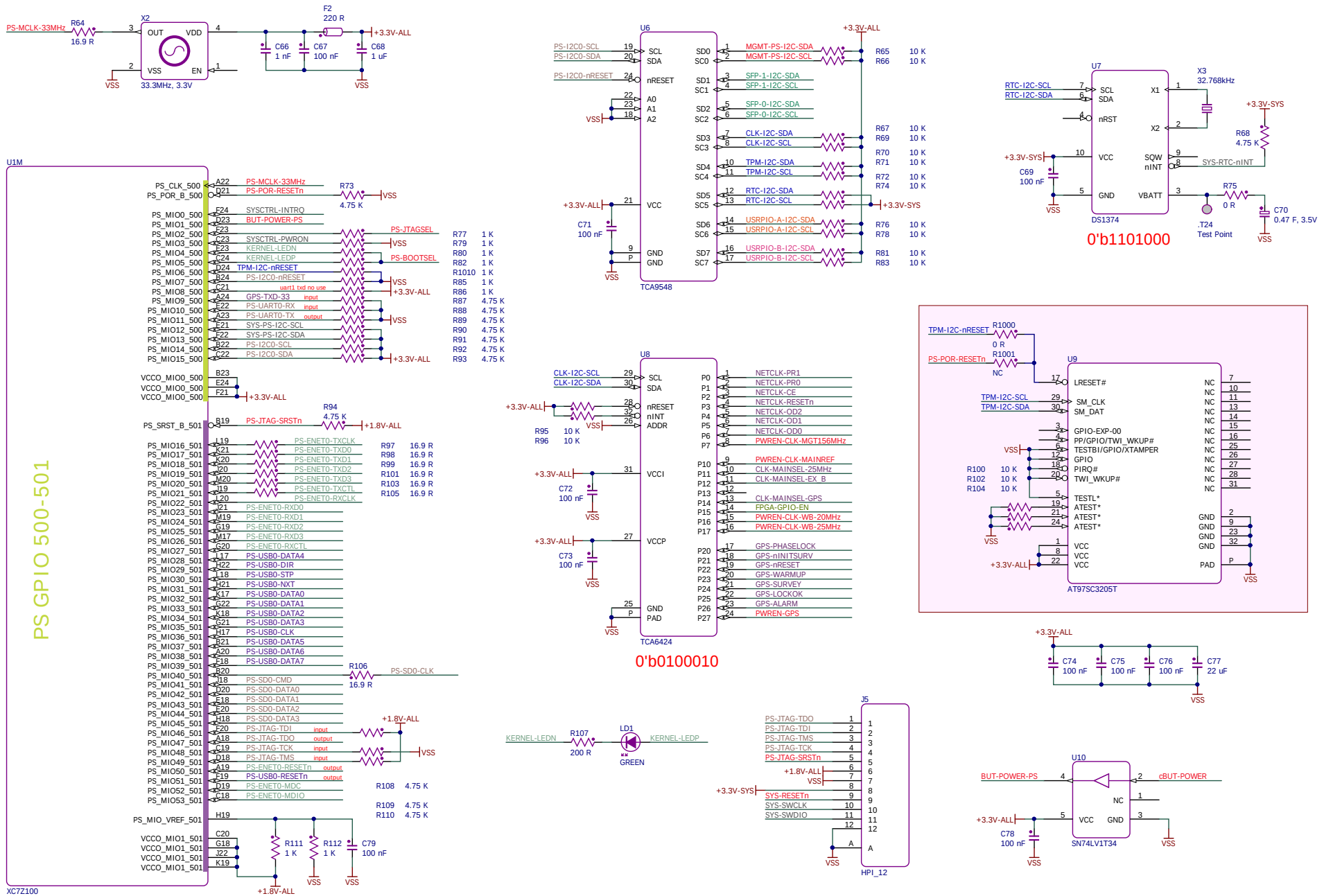
FILE NAME	06_FPGA_MGT.SchDoc	DATE 5/21/2018	SHEET 6 OF 25

159064F-01


PS-MCLK-33MHz
R64
16.9 R
X2
OUT
VDD
VSS
EN
33.3MHz, 3.3V
F2
220 R
C66
1 nF
C67
100 nF
C68
1 uF
+3.3V-ALL
VSS
U1M
PS GPIO 500-501
PS_CLK_500
PS_POR_B_500
PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500
PS-MCLK-33MHz
PS-POR-RESETn
R73
4.75 K
SYSCTRL-INTRQ
BUT-POWER-PS
PS-JTAGSEL
SYSCTRL-PWRON
KERNEL-LEDN
KERNEL-LEDP
PS-BOOTSEL
TPM-I2C-nRESET
PS-I2C0-nRESET
uart1 txd no use
GPS-TXD-33
PS-UART0-RX
PS-UART0-TX
SYS-PS-I2C-SCL
SYS-PS-I2C-SDA
PS-I2C0-SCL
PS-I2C0-SDA
R77 1 K
R79 1 K
R80 1 K
R82 1 K
R1010 1 K
R85 1 K
R86 1 K
R87 4.75 K
R88 4.75 K
R89 4.75 K
R90 4.75 K
R91 4.75 K
R92 4.75 K
R93 4.75 K
VCCO_MIO0_500
VCCO_MIO0_500
VCCO_MIO0_500
PS_SRST_B_501
PS-JTAG-SRSTn
R94
4.75 K
+1.8V-ALL
PS_MIO16_501
PS_MIO17_501
PS_MIO18_501
PS_MIO19_501
PS_MIO20_501
PS_MIO21_501
PS_MIO22_501
PS_MIO23_501
PS_MIO24_501
PS_MIO25_501
PS_MIO26_501
PS_MIO27_501
PS_MIO28_501
PS_MIO29_501
PS_MIO30_501
PS_MIO31_501
PS_MIO32_501
PS_MIO33_501
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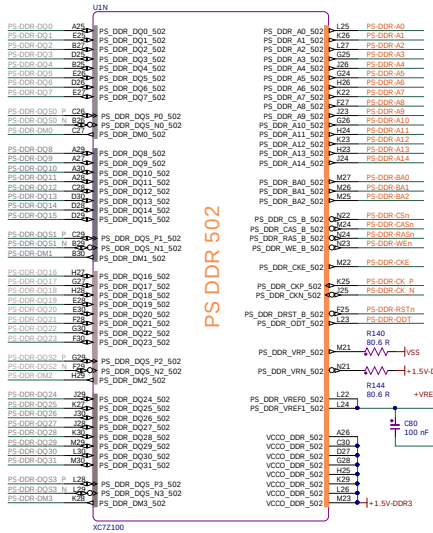
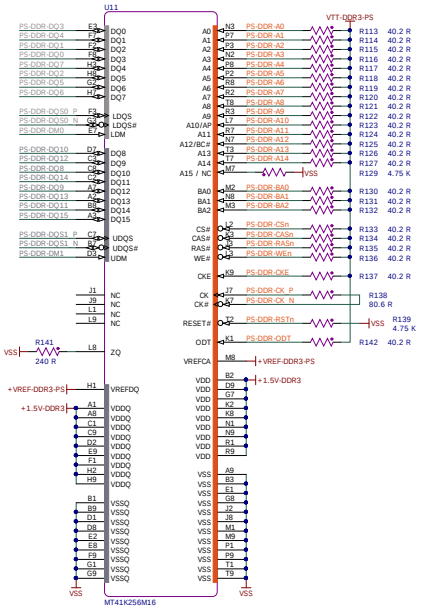
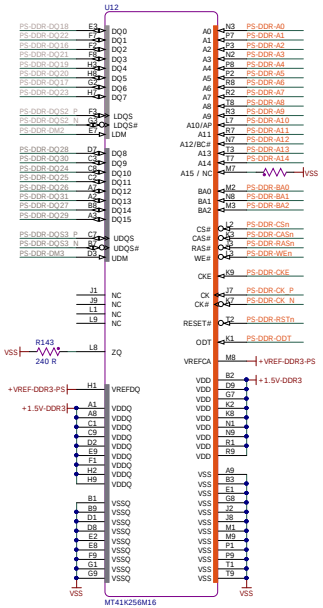
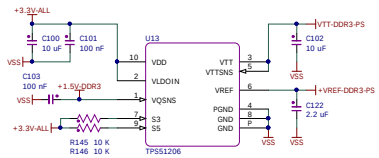
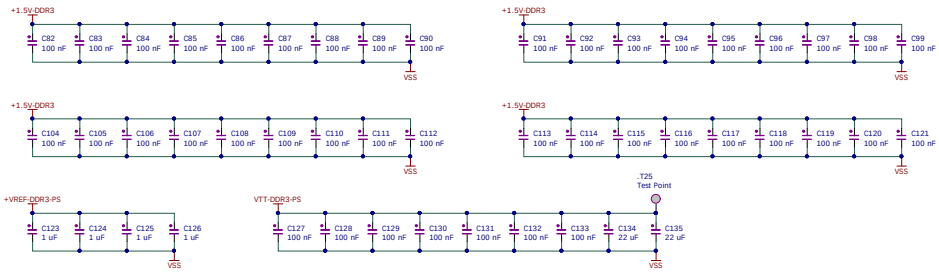
PS_MIO35_501
PS_MIO36_501
PS_MIO37_501
PS_MIO38_501
PS_MIO39_501
PS_MIO40_501
PS_MIO41_501
PS_MIO42_501
PS_MIO43_501
PS_MIO44_501
PS_MIO45_501
PS_MIO46_501
PS_MIO47_501
PS_MIO48_501
PS_MIO49_501
PS_MIO50_501
PS_MIO51_501
PS_MIO52_501
PS_MIO53_501
PS-ENET0-TXCLK
PS-ENET0-TXD0
PS-ENET0-TXD1
PS-ENET0-TXD2
PS-ENET0-TXD3
PS-ENET0-TXCTL
PS-ENET0-RXCLK
PS-ENET0-RXD0
PS-ENET0-RXD1
PS-ENET0-RXD2
PS-ENET0-RXD3
PS-ENET0-RXCTL
PS-USB0-DATA4
PS-USB0-DIR
PS-USB0-STP
PS-USB0-NXT
PS-USB0-DATA0
PS-USB0-DATA1
PS-USB0-DATA2
PS-USB0-DATA3
PS-USB0-CLK
PS-USB0-DATA5
PS-USB0-DATA6
PS-USB0-DATA7
PS-SD0-CLK
PS-SD0-CMD
PS-SD0-DATA0
PS-SD0-DATA1
PS-SD0-DATA2
PS-SD0-DATA3
PS-JTAG-TDI
PS-JTAG-TDO
PS-JTAG-TCK
PS-JTAG-TMS
PS-ENET0-RESETn
PS-USB0-RESETn
PS-ENET0-MDC
PS-ENET0-MDIO
R97 16.9 R
R98 16.9 R
R99 16.9 R
R101 16.9 R
R103 16.9 R
R105 16.9 R
R106
16.9 R
R108 4.75 K
R109 4.75 K
R110 4.75 K
PS_MIO_VREF_501
VCCO_MIO1_501
VCCO_MIO1_501
VCCO_MIO1_501
VCCO_MIO1_501
R111
1 K
R112
1 K
C79
100 nF
XC7Z100
U6
PS-I2C0-SCL
PS-I2C0-SDA
PS-I2C0-nRESET
SCL
SDA
nRESET
A0
A1
A2
VCC
GND
GND
SD0
SC0
SD1
SC1
SD2
SC2
SD3
SC3
SD4
SC4
SD5
SC5
SD6
SC6
SD7
SC7
MGMT-PS-I2C-SDA
MGMT-PS-I2C-SCL
SFP-1-I2C-SDA
SFP-1-I2C-SCL
SFP-0-I2C-SDA
SFP-0-I2C-SCL
CLK-I2C-SDA
CLK-I2C-SCL
TPM-I2C-SDA
TPM-I2C-SCL
RTC-I2C-SDA
RTC-I2C-SCL
USRPIO-A-I2C-SDA
USRPIO-A-I2C-SCL
USRPIO-B-I2C-SDA
USRPIO-B-I2C-SCL
R65 10 K
R66 10 K
R67 10 K
R69 10 K
R70 10 K
R71 10 K
R72 10 K
R74 10 K
R76 10 K
R78 10 K
R81 10 K
R83 10 K
C71
100 nF
TCA9548
U8
CLK-I2C-SCL
CLK-I2C-SDA
nRESET
nINT
ADDR
VCCI
VCCP
GND
PAD
R95 10 K
R96 10 K
C72
100 nF
C73
100 nF
NETCLK-PR1
NETCLK-PR0
NETCLK-CE
NETCLK-RESETn
NETCLK-OD2
NETCLK-OD1
NETCLK-OD0
PWREN-CLK-MGT156MHz
PWREN-CLK-MAINREF
CLK-MAINSEL-25MHz
CLK-MAINSEL-EX_B
CLK-MAINSEL-GPS
FPGA-GPIO-EN
PWREN-CLK-WB-20MHz
PWREN-CLK-WB-25MHz
GPS-PHASELOCK
GPS-nINITSURV
GPS-nRESET
GPS-WARMUP
GPS-SURVEY
GPS-LOCKOK
GPS-ALARM
PWREN-GPS
TCA6424
0'b0100010
U7
RTC-I2C-SCL
RTC-I2C-SDA
SCL
SDA
nRST
VCC
GND
X1
X2
SQW
nINT
VBATT
X3
32.768kHz
R68
4.75 K
SYS-RTC-nINT
R75
0 R
C69
100 nF
C70
0.47 F, 3.5V
.T24
Test Point
DS1374
0'b1101000
U9
TPM-I2C-nRESET
PS-POR-RESETn
R1000
0 R
R1001
NC
LRESET#
TPM-I2C-SCL
TPM-I2C-SDA
SM_CLK
SM_DAT
GPIO-EXP-00
PP/GPIO/TWI_WKUP#
TESTBI/GPIO/XTAMPER
GPIO
PIRQ#
TWI_WKUP#
R100 10 K
R102 10 K
R104 10 K
TESTL*
ATEST*
ATEST*
ATEST*
VCC
VCC
VCC
GND
GND
GND
GND
PAD
AT97SC3205T
C74
100 nF
C75
100 nF
C76
100 nF
C77
22 uF
U10
BUT-POWER-PS
cBUT-POWER
NC
VCC
GND
C78
100 nF
SN74LV1T34
KERNEL-LEDN
R107
200 R
LD1
GREEN
KERNEL-LEDP
J5
PS-JTAG-TDO
PS-JTAG-TDI
PS-JTAG-TMS
PS-JTAG-TCK
PS-JTAG-SRSTn
+1.8V-ALL
SYS-RESETn
SYS-SWCLK
SYS-SWDIO
HPI_12
FPGA PS I/O Assignment / I2C / TPM
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD
SIZE C
DOC CODE 7U296
DRAWING PROJECT NO 159064F-01
REV 1
FILE NAME 07_FPGA_PS_IO.SchDoc
DATE 5/21/2018
SHEET 7 OF 25











FPGA PS DDR3 Memory			
SCH, USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
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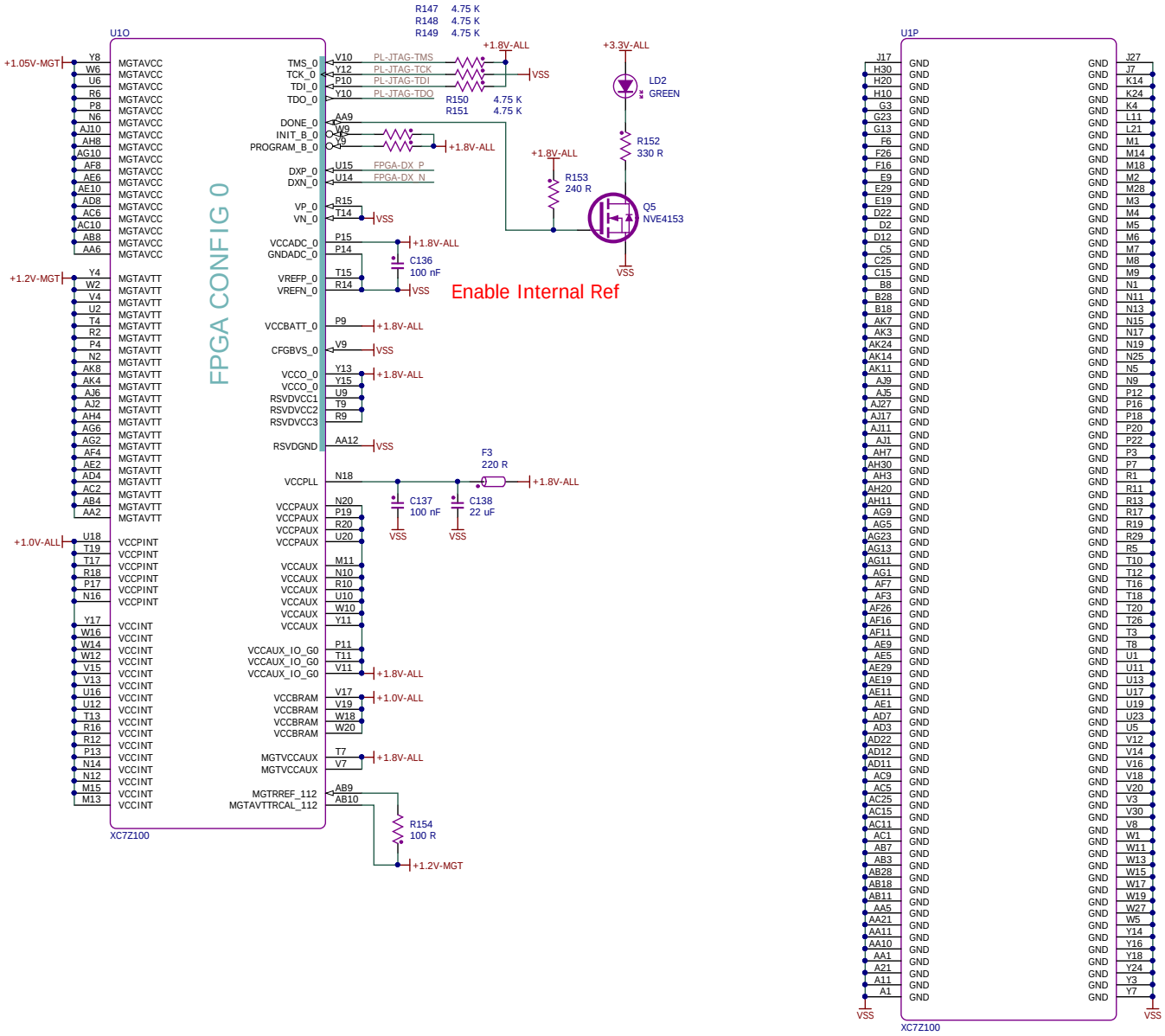
FILE NAME	08_FPGA_PS_DDR.SchDoc	DATE 5/21/2018	SHEET 8 OF 25



FPGA Power and Configuration			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
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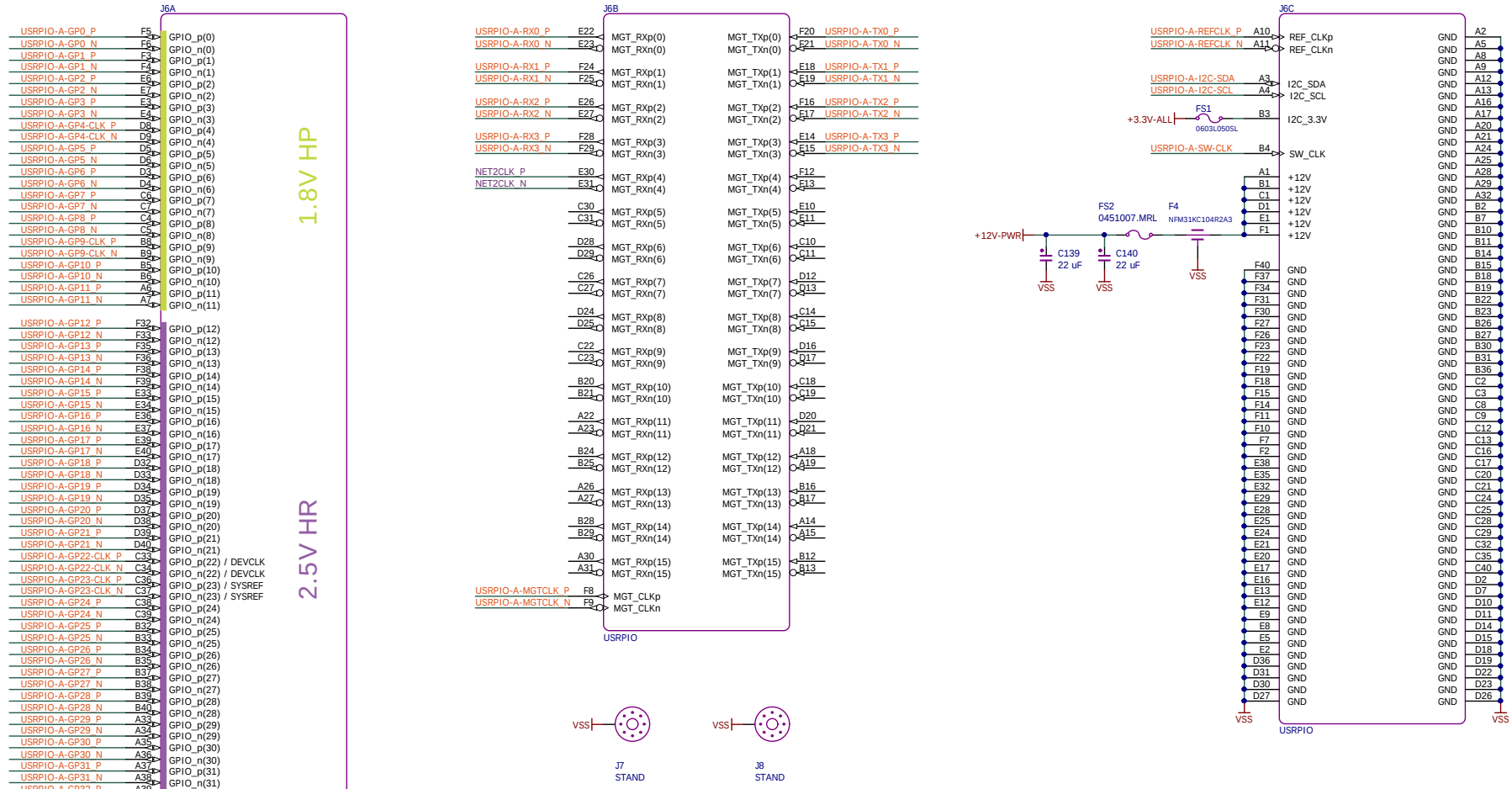
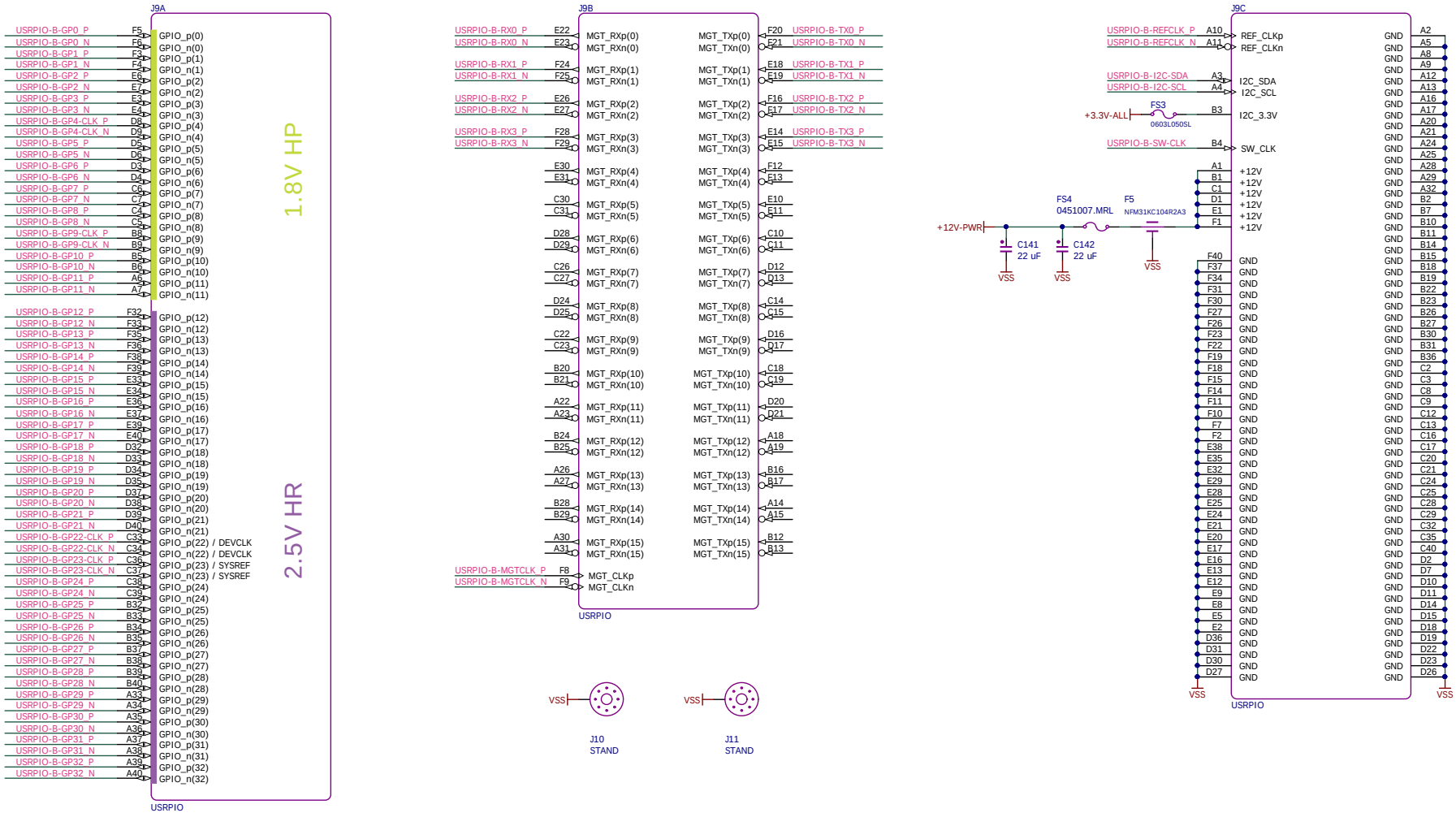
FILE NAME	09_FPGA_Config.SchDoc	DATE 5/21/2018	SHEET 9 OF 25

159064F-01



USRPIO Channel A			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	10_USRPIO_A.SchDoc	DATE 5/21/2018	SHEET 10 OF 25

159064F-01



USRPIO Channel B			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
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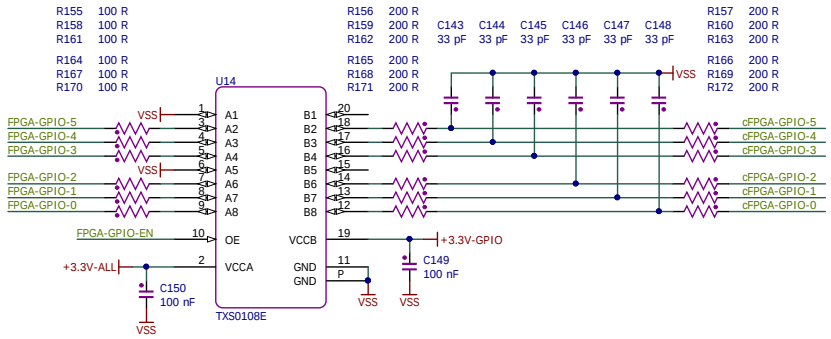
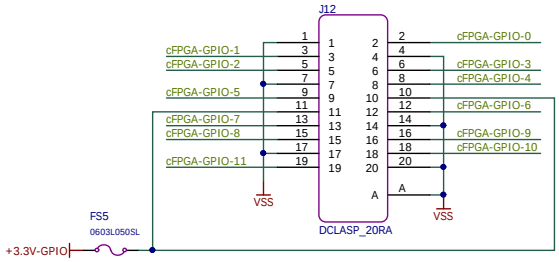
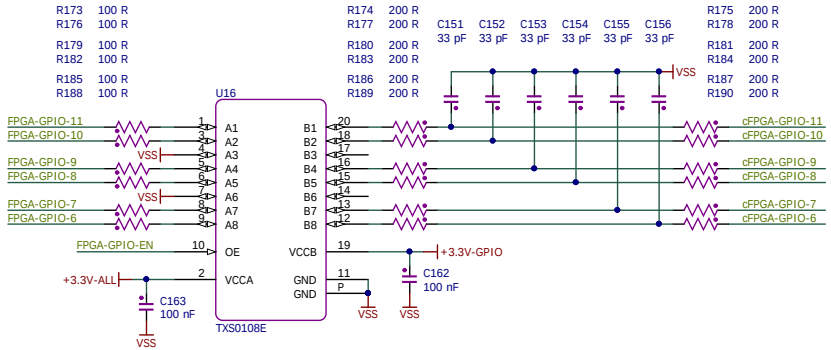
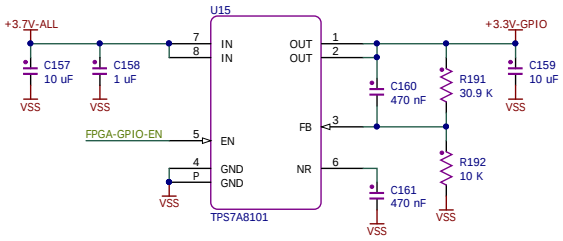
FILE NAME	11_USRPIO_B.SchDoc	DATE 5/21/2018	SHEET 11 OF 25

159064F-01









GPIO Interface			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
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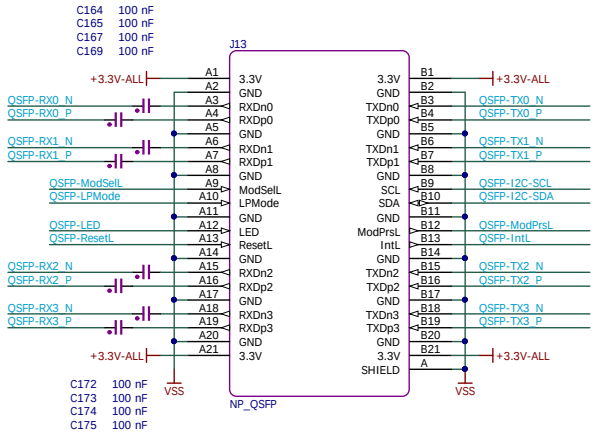
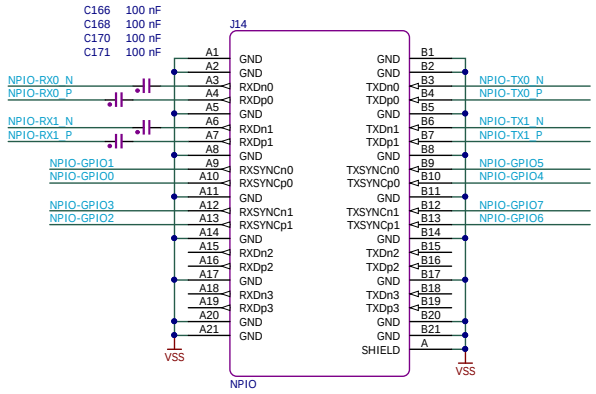
FILE NAME	12_GPIO.SchDoc	DATE 5/21/2018	SHEET 12 OF 25

159064F-01





Nano pitch IO Interface			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
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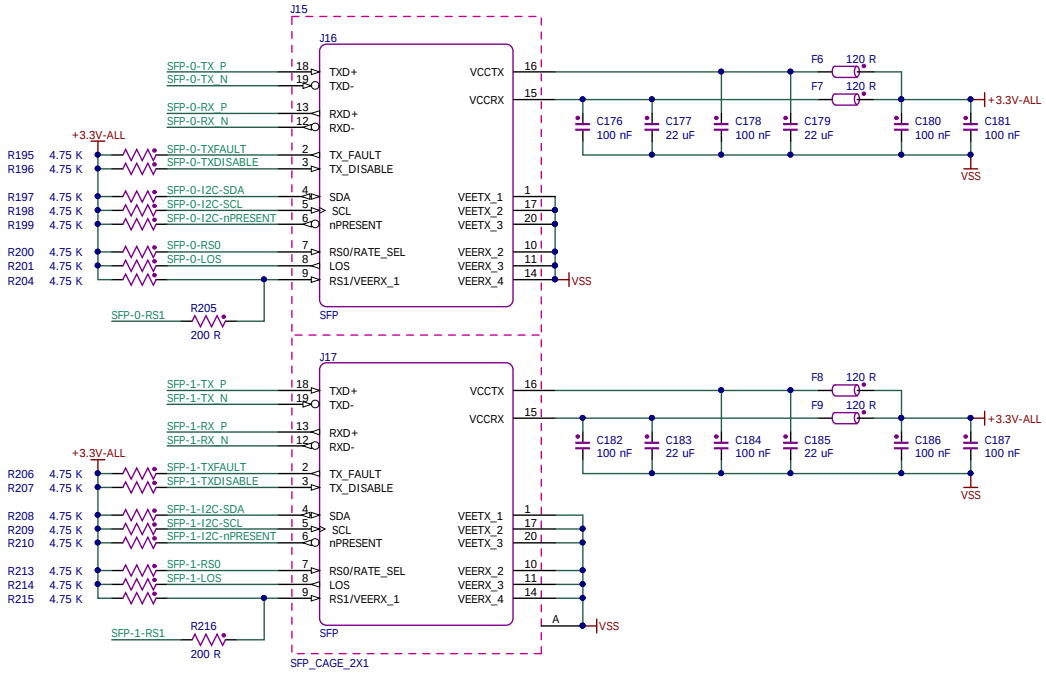
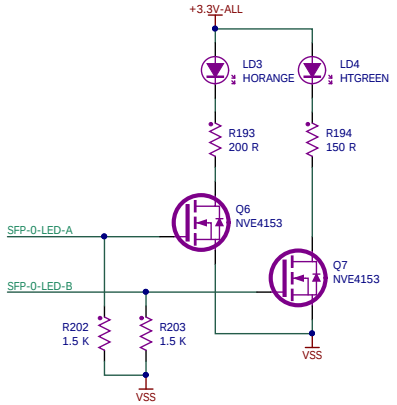
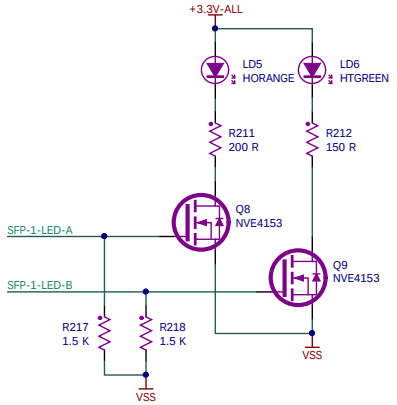
FILE NAME: 13_NPIO.SchDoc		DATE: 5/21/2018	SHEET 13 OF 25

159064F-01







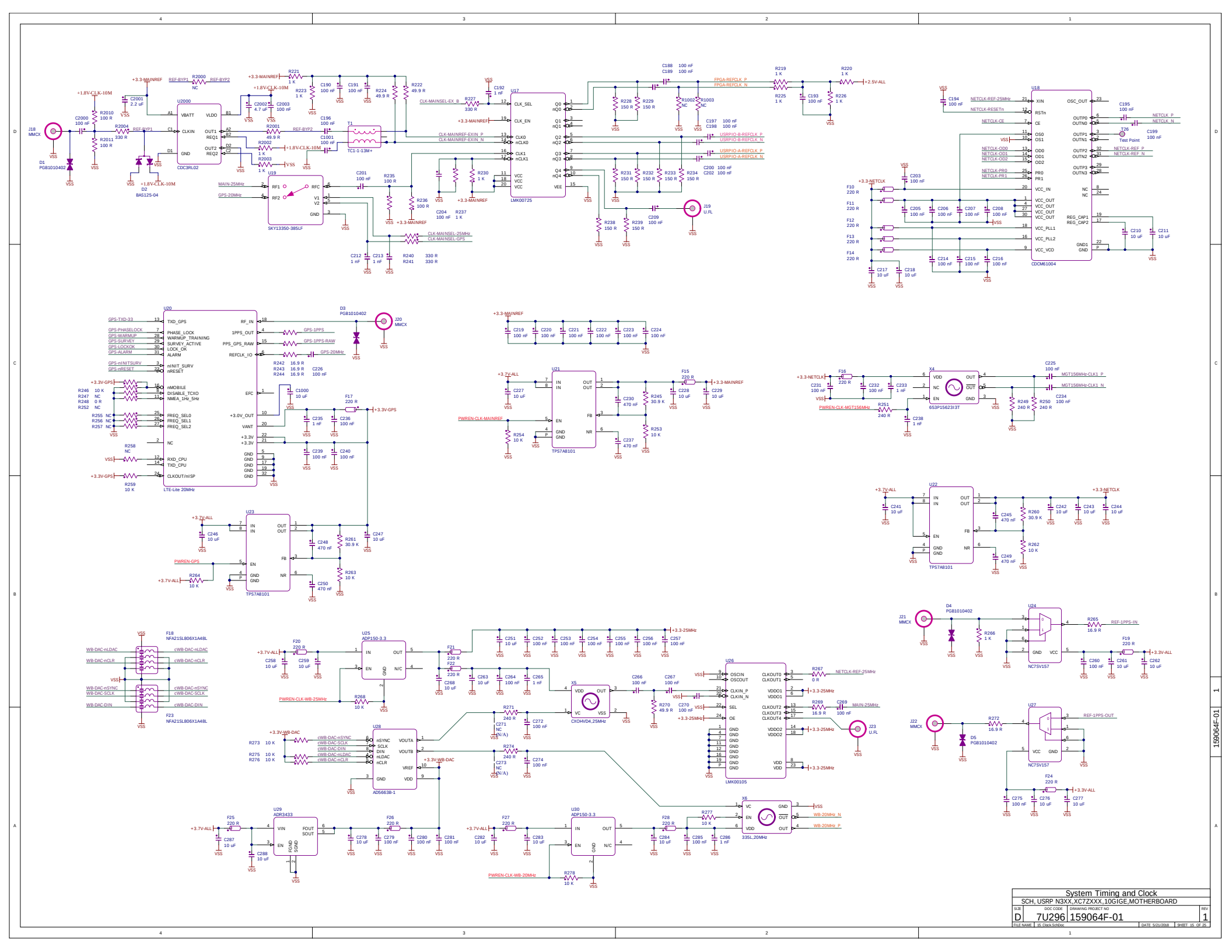
SFP+ Interface

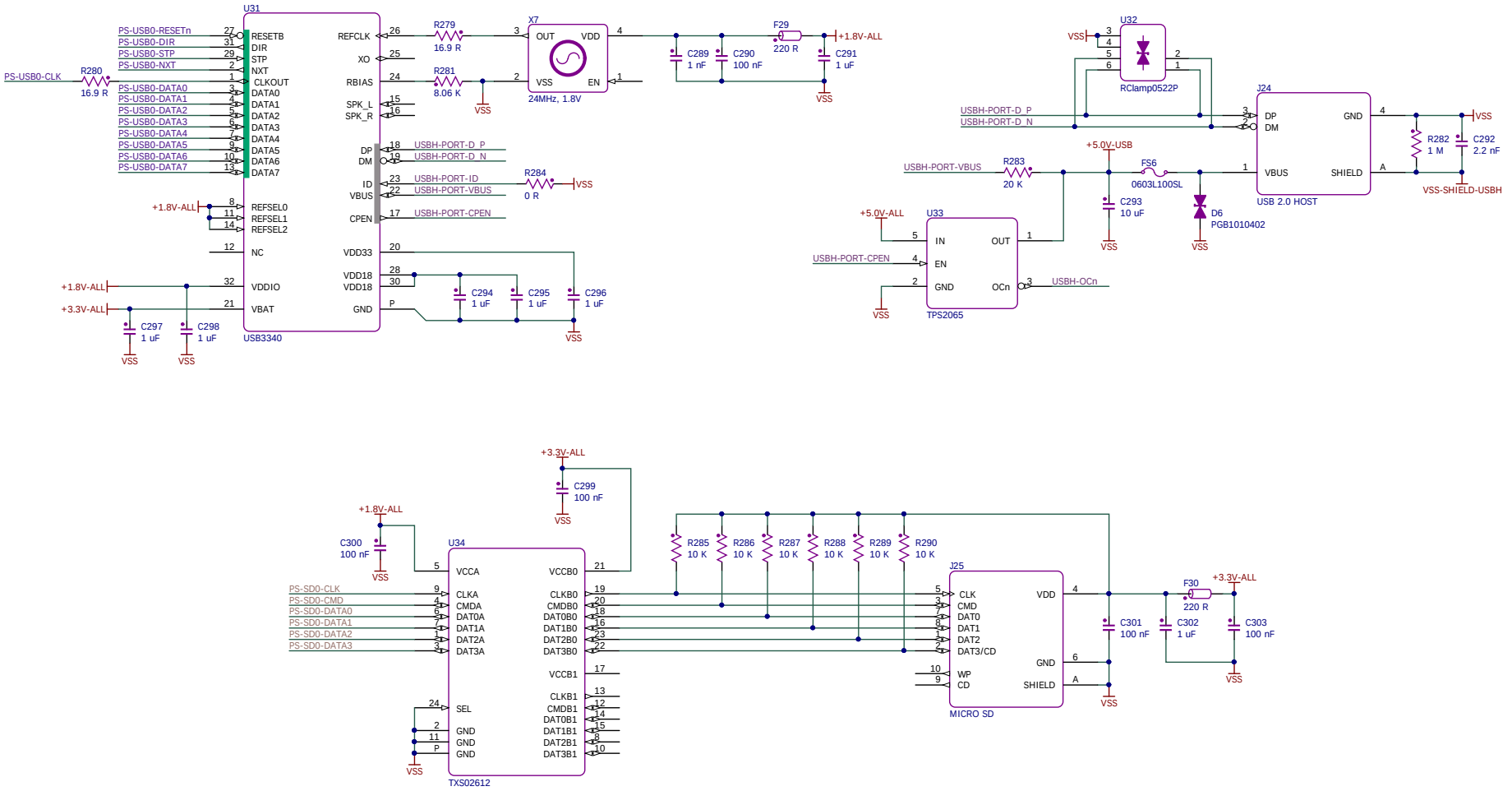
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD

SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1

FILE NAME	DATE	SHEET
14_SFP.SchDoc	5/21/2018	14 OF 25

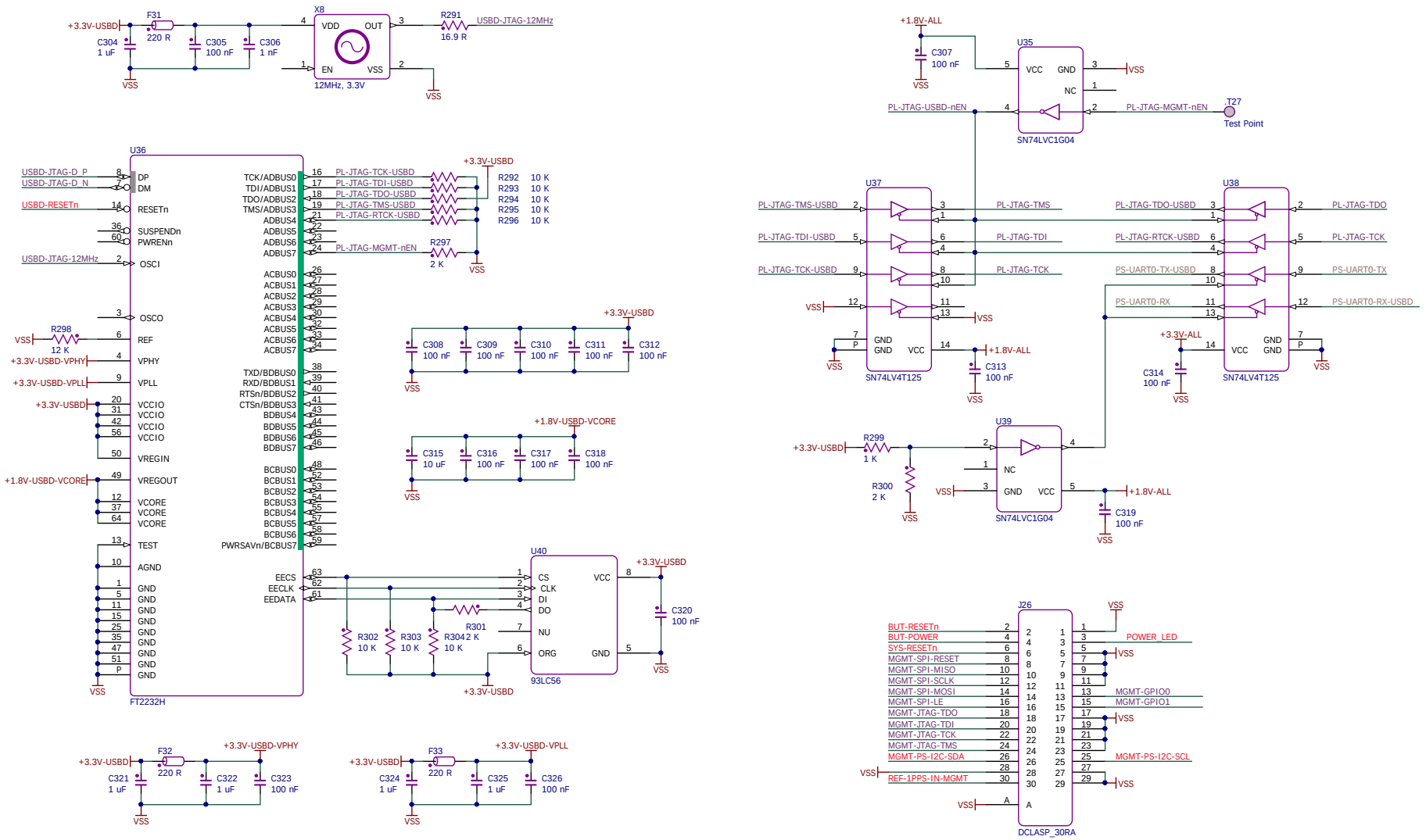
159064F-01


U2000
CDC3RL02
U17
LMK00725
U18
CDCM61004
U19
SKY13350-385LF
U20
LTE-Lite 20MHz
U21
TPS7A8101
U22
TPS7A8101
U23
TPS7A8101
U24
NC7SV157
U25
ADP150-3.3
U26
LMK00105
U27
NC7SV157
U28
AD5663B-1
U29
ADR3433
U30
ADP150-3.3
X4
653P156231ST
X5
CXOHVD4,25MHz
X6
335L,20MHz
T1
TC1-1-13M+
D1
PGB1010402
D2
BAS125-04
D3
PGB1010402
D4
PGB1010402
D5
PGB1010402
J18
MMCX
J19
U.FL
J20
MMCX
J21
MMCX
J22
MMCX
J23
U.FL
T26
Test Point
+1.8V-CLK-10M
+3.3-MAINREF
+2.5V-ALL
+3.3V-NETCLK
+3.3V-GPS
+3.7V-ALL
+3.3-WB-DAC
+3.3-25MHz
MAIN-25MHz
GPS-20MHz
NETCLK-REF-25MHz
NETCLK-RESETn
NETCLK-CE
NETCLK-OD0
NETCLK-OD1
NETCLK-OD2
NETCLK-PR0
NETCLK-PR1
FPGA-REFCLK_P
FPGA-REFCLK_N
USRPIO-B-REFCLK_P
USRPIO-B-REFCLK_N
USRPIO-A-REFCLK_P
USRPIO-A-REFCLK_N
CLK-MAINSEL-EX_B
CLK-MAINREF-EXIN_P
CLK-MAINREF-EXIN_N
CLK-MAINSEL-25MHz
CLK-MAINSEL-GPS
MGT156MHz-CLK1_P
MGT156MHz-CLK1_N
PWREN-CLK-MGT156MHz
PWREN-CLK-MAINREF
PWREN-GPS
PWREN-CLK-WB-25MHz
PWREN-CLK-WB-20MHz
WB-DAC-nLDAC
WB-DAC-nCLR
WB-DAC-nSYNC
WB-DAC-SCLK
WB-DAC-DIN
WB-20MHz_N
WB-20MHz_P
REF-1PPS-IN
REF-1PPS-OUT
GPS-TXD-33
GPS-PHASELOCK
GPS-WARMUP
GPS-SURVEY
GPS-LOCKOK
GPS-ALARM
GPS-nINITSURV
GPS-nRESET
GPS-1PPS
GPS-1PPS-RAW
GPS-20MHz
REF-BYP1
REF-BYP2
System Timing and Clock
SCH, USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD
SIZE D
DOC CODE 7U296
DRAWING PROJECT NO 159064F-01
REV 1
FILE NAME 15_Clock.SchDoc
DATE 5/21/2018
SHEET 15 OF 25

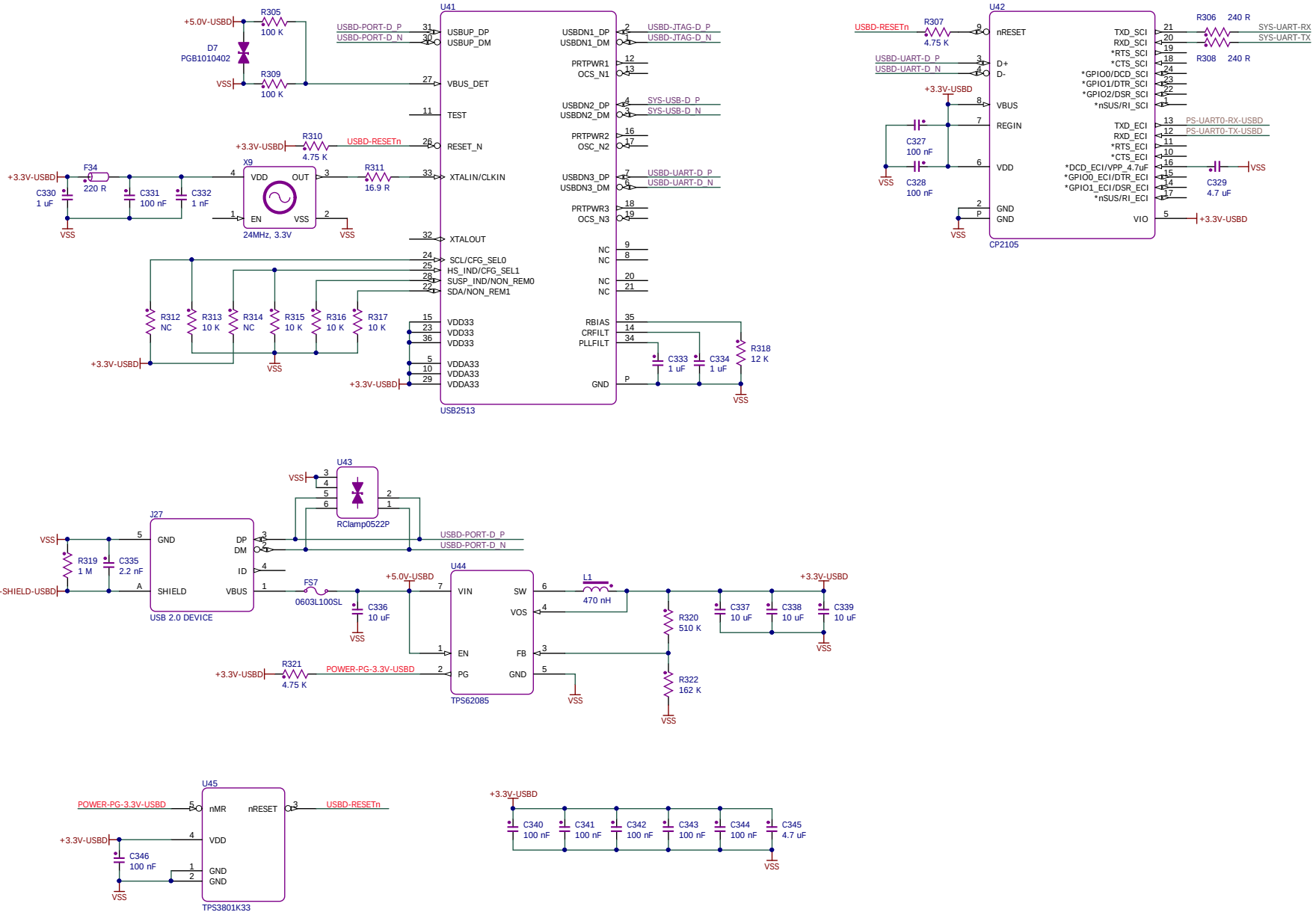


USB 2.0 Host / MicroSD			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 16_USBHost_MicroSD.SchDoc		DATE: 5/21/2018	SHEET 16 OF 25

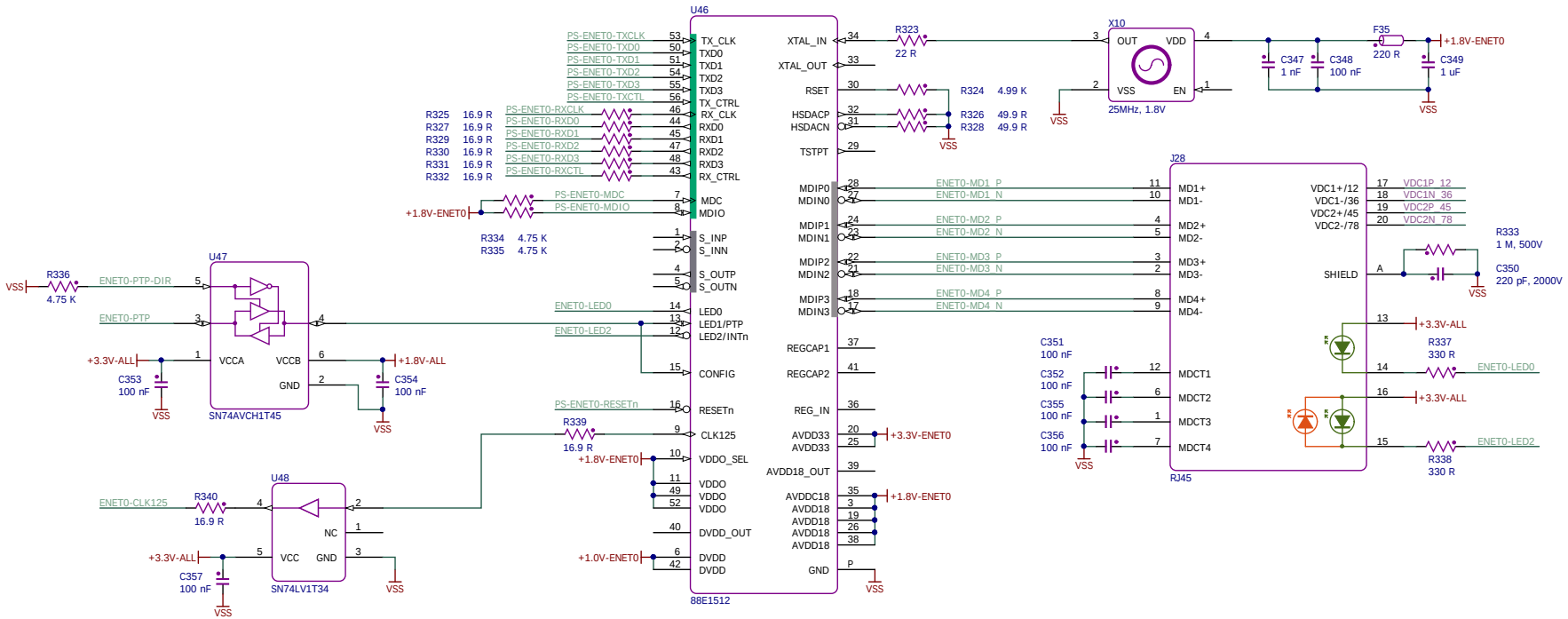
159064F-01



USB JTAG and USB UART for Debug			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	17_USB_Debug.SchDoc	DATE 5/21/2018	SHEET 17 OF 25

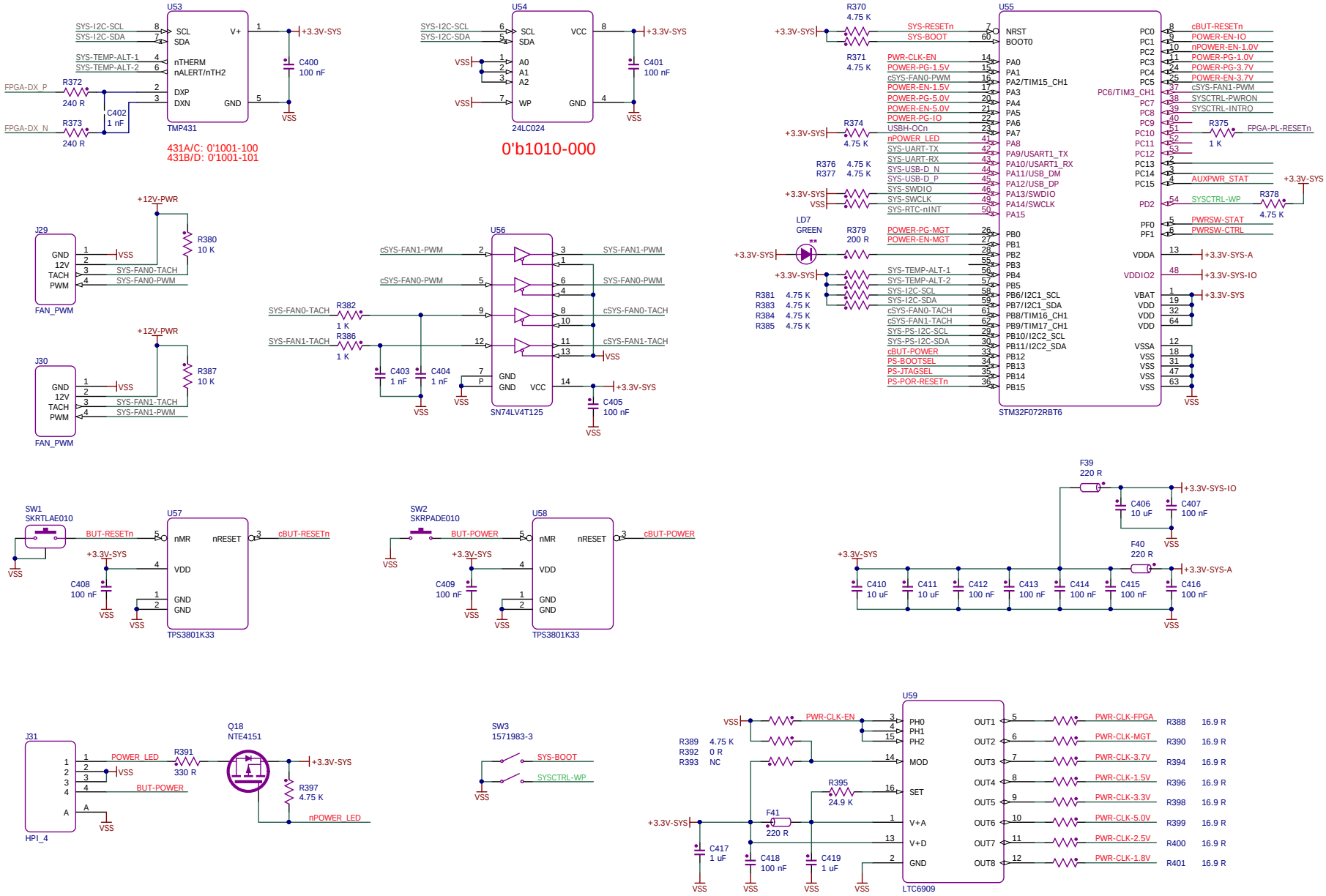


USB 2.0 Hub for Debug Interface			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	18_USB_Hub.SchDoc	DATE 5/21/2018	SHEET 18 OF 25

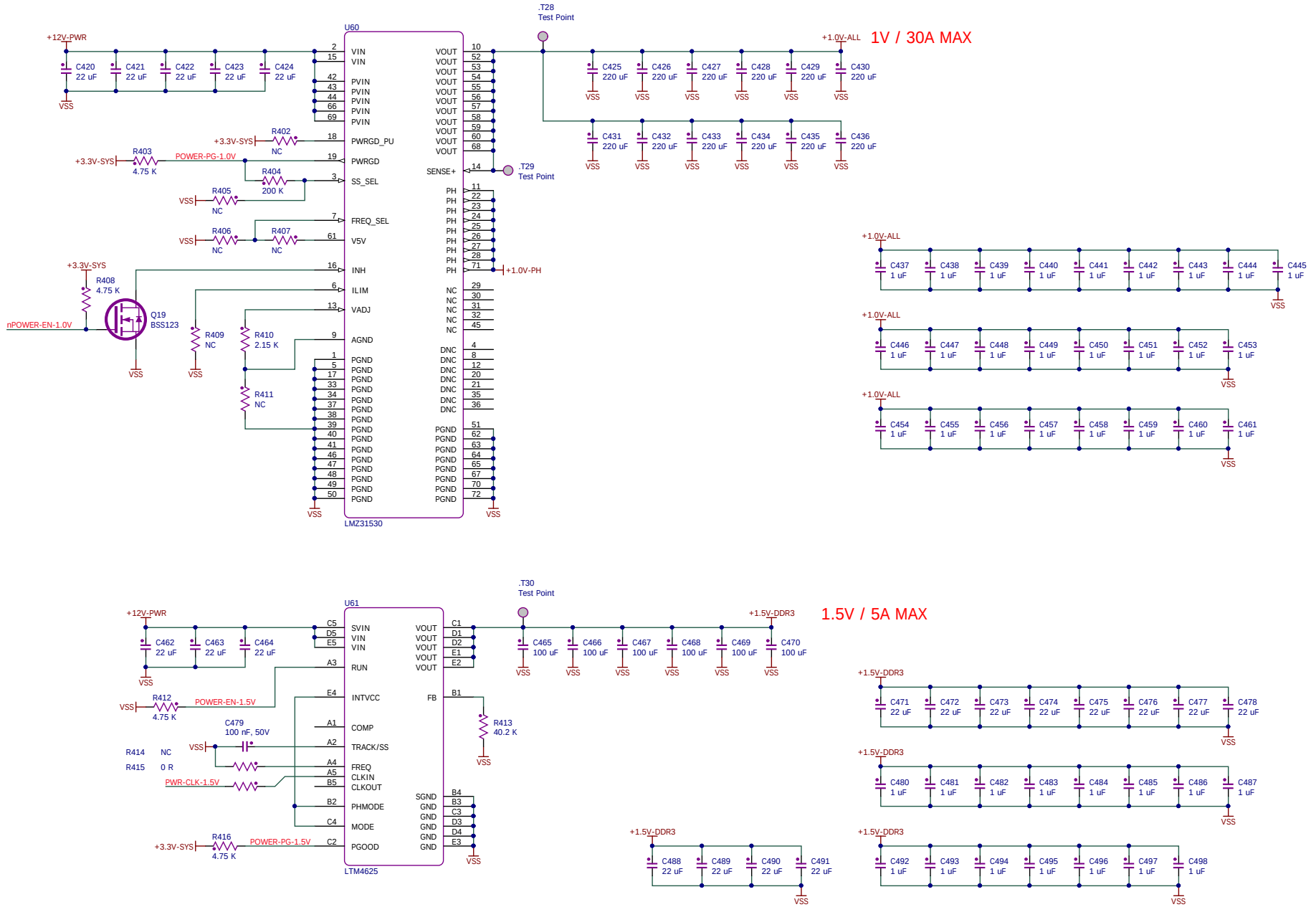


GbE Ethernet Controller and RJ45 Connector			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	19_Ethernet_Controller.SchDoc	DATE 5/21/2018	SHEET 19 OF 25

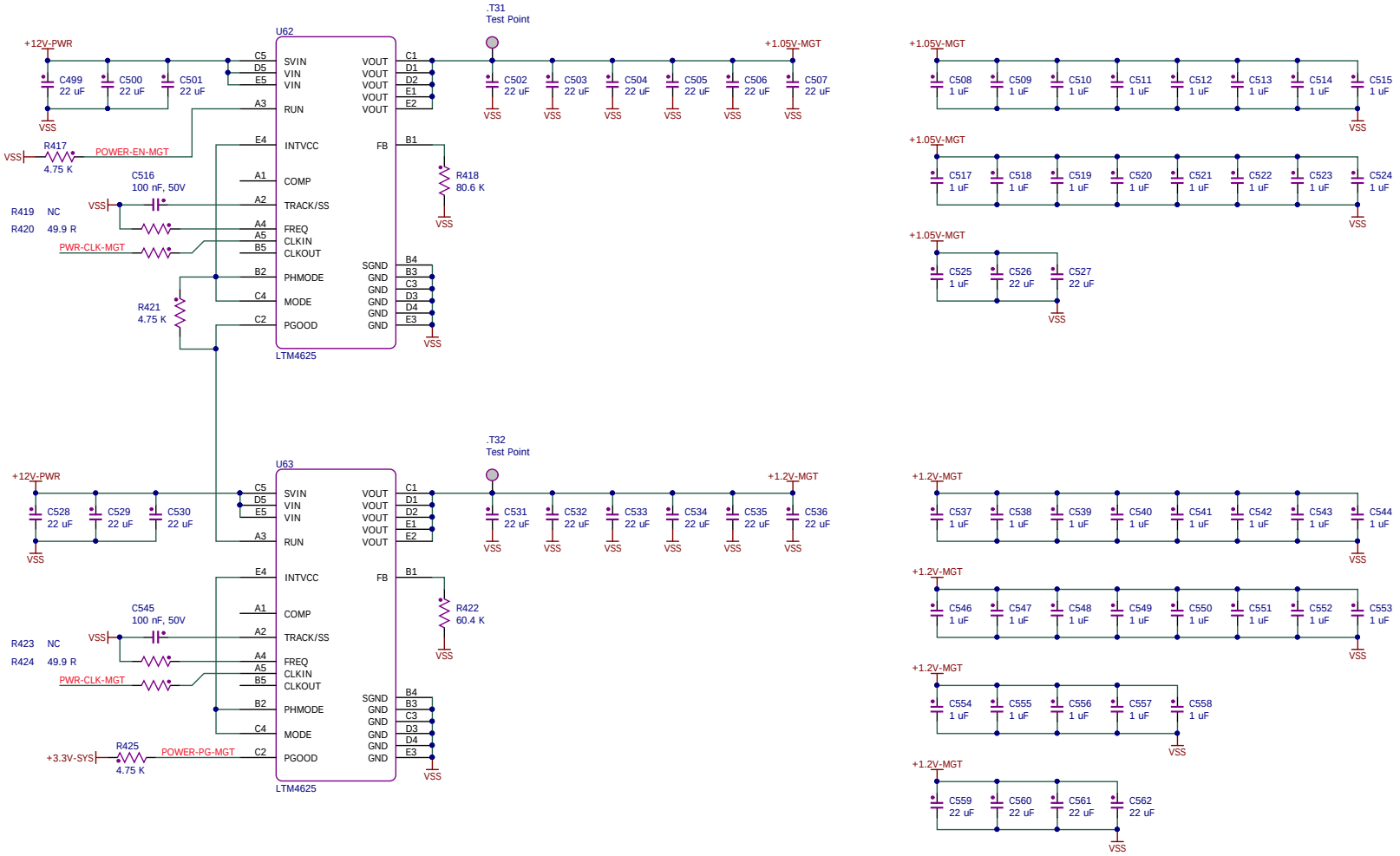
159064F-01



System Controller			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	21_SYSCTRL.SchDoc	DATE 5/21/2018	SHEET 21 OF 25

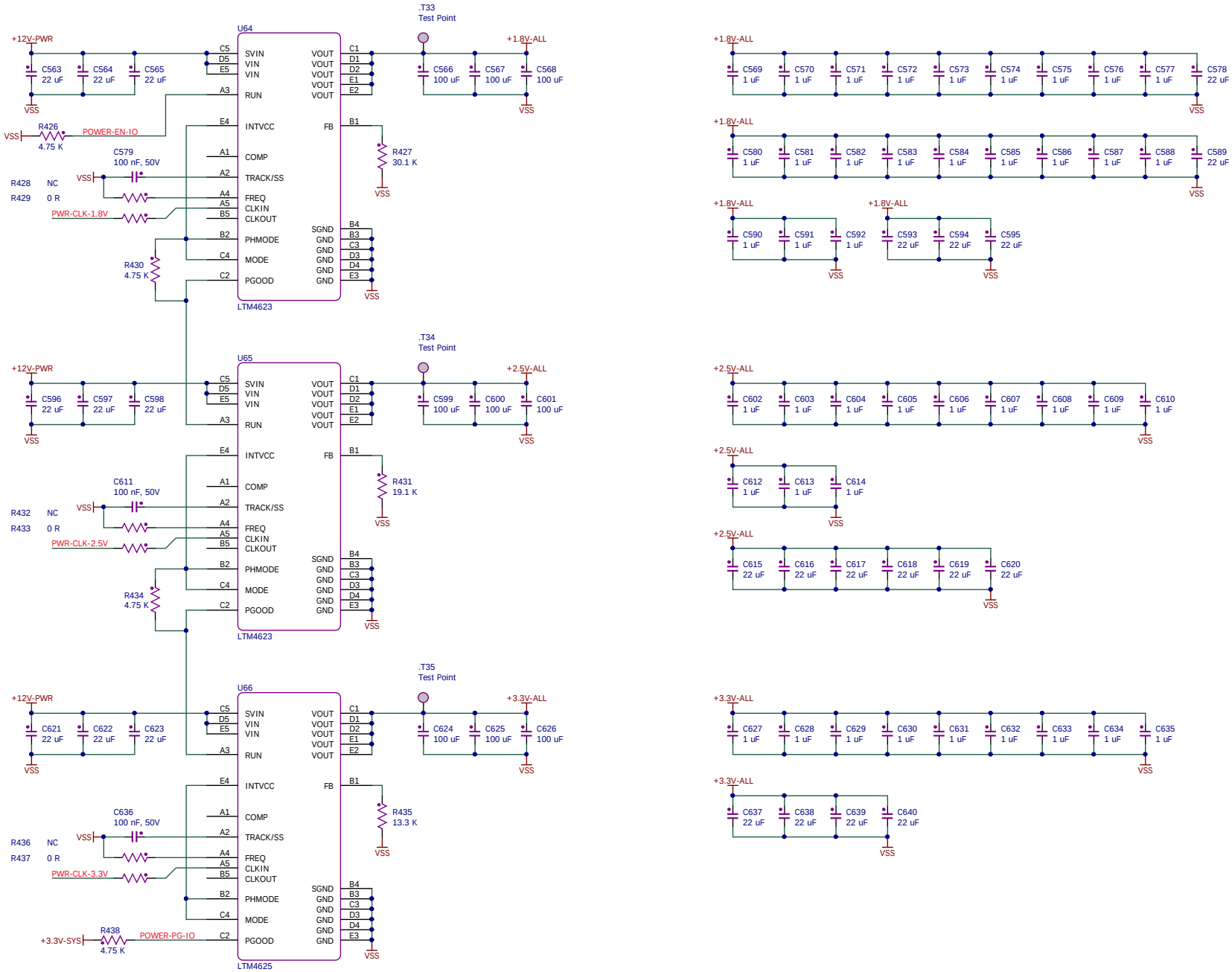


Power Converter Part A			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	22_POWER_A.SchDoc	DATE 5/21/2018	SHEET 22 OF 25

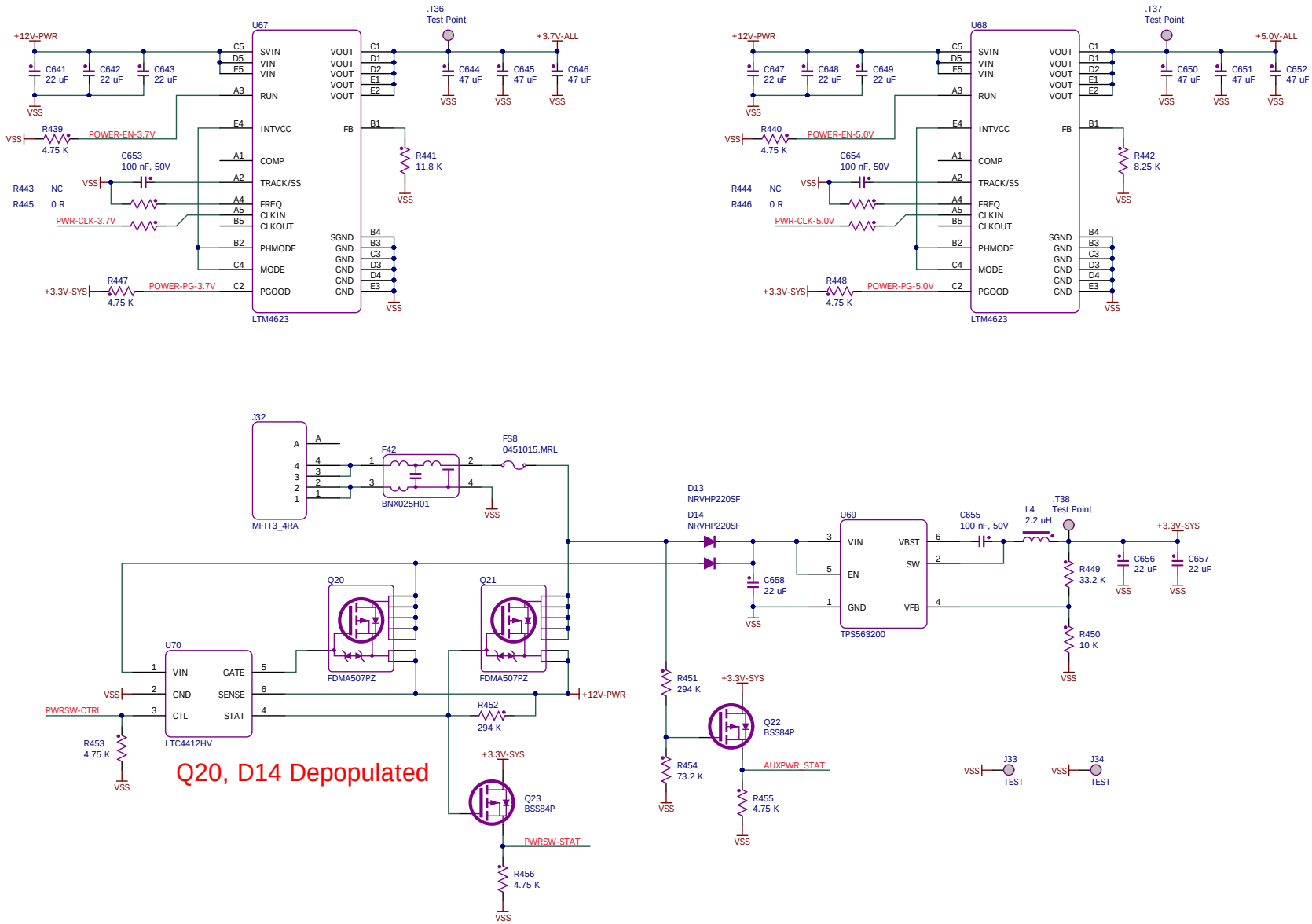


Power Converter Part B			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 23_POWER_B.SchDoc		DATE: 5/21/2018	SHEET 23 OF 25

159064F-01



Power Converter Part C			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE: C	DOC CODE: 7U296	DRAWING PROJECT NO: 159064F-01	REV: 1
FILE NAME: 24_POWER_C.SchDoc		DATE: 5/21/2018	SHEET 24 OF 25



Power Converter Part D			
USRP N3XX,XC7ZXXX,10GIGE,MOTHERBOARD			
SIZE	DOC CODE	DRAWING PROJECT NO	REV
C	7U296	159064F-01	1
FILE NAME	25_POWER_D.SchDoc	DATE 5/21/2018	SHEET 25 OF 25