# About USRP Bandwidths and Sampling Rates

## Contents



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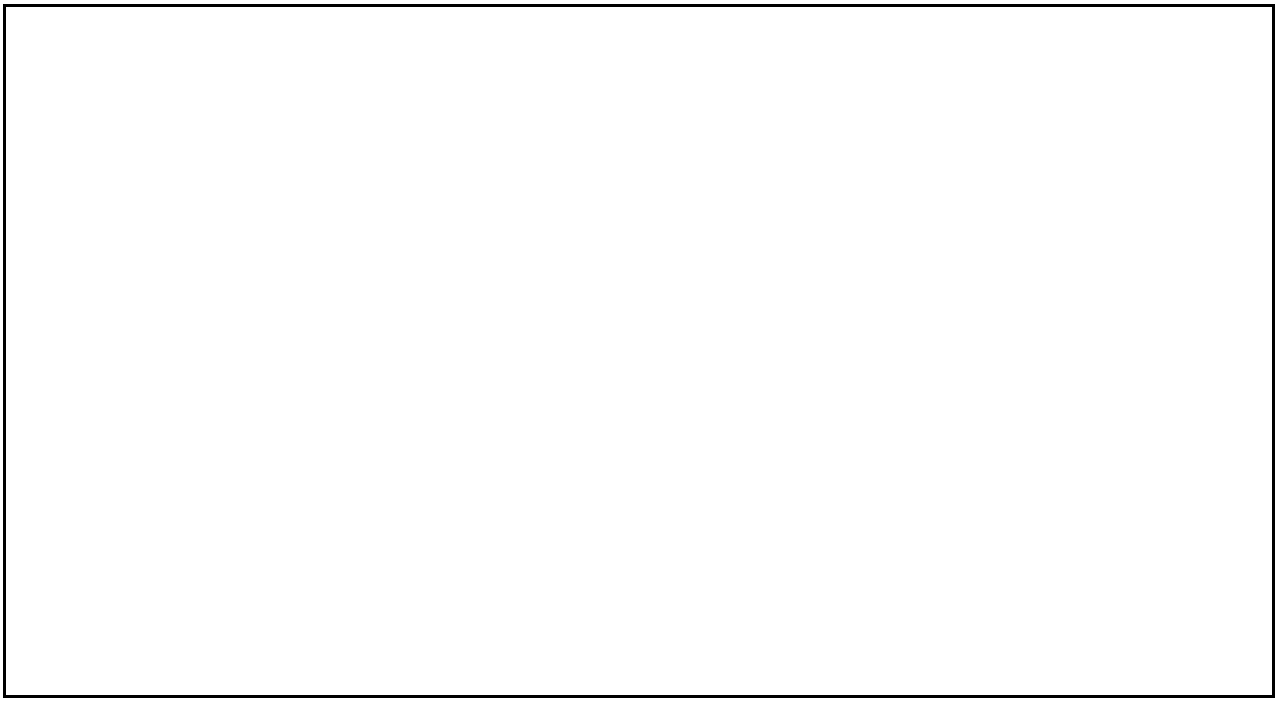
This AN provides insight into the topics of USRP architecture, system bandwidth, host interface throughput, and available sampling rates.


"What is the bandwidth of the USRP? device?" is a commonly asked question. This document will provide some insight into the USRP ? architecture, and how to calculate system bandwidth by analyzing the performance of each part of the signal chain. Common terms such as "analog bandwidth" and "host bandwidth" will be defined. This document requires basic understanding of the Nyquist-Shannon sampling theorem.

While some characteristics and specifications vary from model to model, all USRP devices use the same general architecture. In many cases, the RF frontend, the mixers, filters, oscillators and amplifiers required to translate a signal from the RF domain and the complex baseband or IF signals. The baseband of IF signals are sampled by ADCs, and the digital samples are clocked into an FPGA. The stock FPGA image provides digital down-conversion, functionality, which includes fine-frequency tuning and several filters for decimation. After decimation, raw samples or other data are streamed to a host computer through the host interface. The reverse process applies to the transmit chain.

The bandwidth of the USRP device varies at each point in the signal chain. Three general types of bandwidth specifications are the analog bandwidth, the FPGA processing bandwidth, and host bandwidth. The system bandwidth is generally the minimum of the RF daughterboard, FPGA processing, and host bandwidth. Care should also be taken to avoid an analog bandwidth that is greater than the ADC/DAC sample rate of any device.



The analog bandwidth is the amount of useful bandwidth (3 dB) between the RF port and IF/baseband interface of an RF channel. Typically this bandwidth is set by IF or baseband filters on the daughterboard, which are designed to avoid aliasing when paired with a USRP motherboard with given ADC/DAC sample rates.

| Daughterboard | Frequency Coverage | Analog Bandwidth |
|---|---|---|
| WBX-120 | 50 MHz - 2.2 GHz | 120 MHz |
| SBX-120 | 400 MHz - 4.4 GHz | 120 MHz |
| CBX-120 | 1.2 GHz - 6 GHz | 120 MHz |
| UBX-160 | 10 MHz - 6 GHz | 160 MHz |
| WBX | 50 MHz - 2.2 GHz | 40 MHz |
| SBX | 400 MHz - 4.4 GHz | 40 MHz |

| | | |
|---|---|---|
| CBX | 1.2 GHz - 6 GHz | 40 MHz |
| UBX-40 | 10 MHz - 6 GHz | 40 MHz |
| TVRX2 | 50 MHz - 860 MHz | Configurable ? 1.7 to 10 MHz |
| DBSRX2 | 800 MHz ? 2.3 GHz | Configurable ? 8 to 80 MHz |
| BasicRX / BasicTX | 1 ? 250 MHz | *Determined by ADC/DAC sample rates. External filter required. |
| LFRX / LFTX | DC-30 MHz | 30 MHz |

The FPGA processing bandwidth is the sample rate provided by the ADCs and DACs on the USRP motherboard. This sets the hypothetical maximum digital bandwidth of a system based on the USRP. For example, the FPGA of the USRP X300/X310 sends and receives samples at 200 MS/s from the DACs and ADCs respectively. The stock FPGA design of all USRP devices include DSP chains that provide frequency shifting, decimation of received streams, and interpolated of transmit streams. These DSP chains operate at the specified FPGA processing bandwidth.

- Note: Users that customize the FPGA may incorporate their own, custom DSP functionality. Given the large number of design factors involved in FPGA design, these specifications do not guarantee that custom DSP functions will run at the full rate.

| USRP ? Model | ADC Processing Bandwidth (MS/s) | DAC Processing Bandwidth (MS/s) |
|---|---|---|
| USRP B200mini / USRP B205mini / USRP B206mini | 61.44 MS/s (simplex) | 61.44 MS/s (simplex) |
| USRP B200 / USRP B210 | 61.44 MS/s (simplex) | 61.44 MS/s (simplex) |
| USRP E310 / USRP E312 | 61.44 MS/s (simplex) | 61.44 MS/s (simplex) |
| USRP N200 / USRP N210 | 100 MS/s | 400 MS/s |
| USRP X300 / USRP X310 | 200 MS/s | 800 MS/s |

The host interface allows data to stream between the FPGA of a USRP device, and a host PC. Most applications stream I/Q data to and from the USRP device. A summary of the various interface options that are available with the USRP product line are shown below. The host sample rate with 16-bit I&Q samples are shown. Most USRP models also provide to option to stream 8-bit samples, effectively doubling the host-bandwidth in terms of samples/second.

In this context, "full duplex" means that the interface can stream in both directions at the specified rates simultaneously. Some interfaces, such as USB 3.0, do not provide separate data paths for transmit and receive data, but reuse a single transport in a "half duplex" mode. In this case, the total interface bandwidth would be shared between the transmit and receive functions of a USRP.

- Note: The actual streaming performance will depend on the processing capability of the host computer, the complexity of the application/DSP, and other factors. This table merely represents the maximum theoretical throughput of each host interface.

| Interface | USRP ? Devices | Host Sample Rate (MS/s @ 16-bit I/Q) | Half/Full Duplex |
|---|---|---|---|
| USB 2.0 | USRP ? 1, B100 | 8 | Half Duplex |
| USB 3.0 | B200/210/200mini/205mini/206mini | 61.44 | Half Duplex |
| Gigabit Ethernet | N200/N210 | 25 | Full Duplex |
| 10 Gigabit Ethernet | X300/X310 | 200 | Full Duplex |
| PCI-Express (4-lane PCIe Card) | X300/X310 | 200 | Full Duplex |
| PCI-Express (1-lane ExpressCard) | X300/X310 | 50 | Full Duplex |
| OMAP GPMC | E100/E110 | 4 | Half Duplex |

** Caution: Use of wide bandwidth daughterboards with lower bandwidth USRP? devices will result in aliasing.*

It is important to meet filtering and bandwidth requirements to avoid aliasing. The extended bandwidth WBX-120, CBX-120 and SBX-120 daughterboards were design to work with USRP X300/X310 and any future products with sufficient ADC/DAC sample rates. These boards are not compatible with devices that incorporate lower rate ADC/DAC below 200 MS/s. See "Daughterboard Compatibility" for more information.

The bandwidth of the USRP-based system depends on the specific implementation and functional allocation.

- Example 1:A system that uses a USRP X300/X310 with a 10 GigE interface, a fully host-based application, and a 40 MHz daughterboard will provide a usable bandwidth of 40 MHz. The limit is set by the daughterboard.
- Example 2: A system that uses a USRP N200/N210 with a 1 GigE interface, a fully host-based application that requires 16-bit samples, and a 40 MHz daughterboard will provide a useable bandwidth of ~20 MHz. The limit is set by the host interface ? 1 GigE can stream up to 25 MS/s, which translates to ~20 MHz of usable bandwidth.
- Example 3: A system that uses a USRP X300/X310 with a 1 GigE interface for command/control, full FPGA processing of the rx/tx steams, and a 120 MHz daughterboard may provide usable bandwidth up to 120 MHz. The FPGA can process samples at 200 MS/s. The daughterboard is the limiting factor.