Aurora

The Aurora FPGA image (AA) is built with the free Xilinx Aurora FPGA-IP, allowing for FPGA to FPGA high speed serial link. Think of Aurora as a link-layer transport protocol, providing a programming interface for the user application to use to do actual data transport. Aurora was used in the DARPA SC2 Colosseum for high-speed transfer between Ettus USRPs and other FPGA processing devices. Aurora removes the internet protocol layers, providing direct access to the physical networking interface: bits in, bits out ... no overhead for ethernet, IP, UDP! The UHD manual provide a little information about the Aurora FPGA images for various USRPs:

- E320
  - https://files.ettus.com/manual/page_usrp_e3xx.html#e320_fpga_flavours
  - https://files.ettus.com/manual/page_usrp_e3xx.html#e3xx_troubleshooting_bist]
- N300/N310 and N320/N321
  - https://files.ettus.com/manual/page_usrp_n3xx.html#n3xx_getting_started_fpga_update_flavors
  - https://files.ettus.com/manual/page_usrp_n3xx.html#n3xx_troubleshooting_bist
  - https://files.ettus.com/manual/page_usrp_n3xx.html#n3xx_mg_regmap
  - https://files.ettus.com/manual/page_usrp_n3xx.html#n3xx_rh_sfp_protocols