

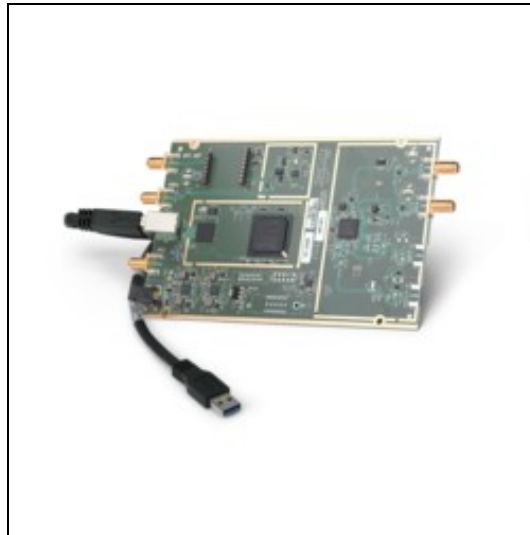
B205mini

Contents

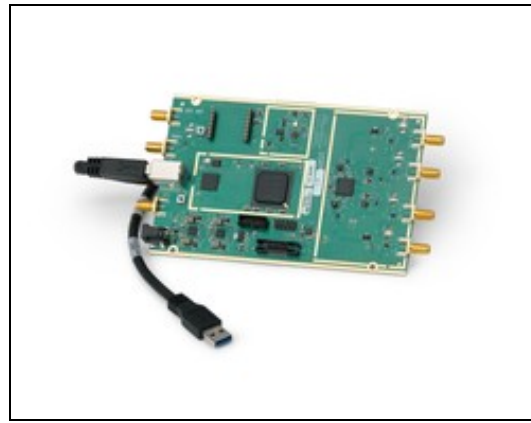
- 1 Device Overview
- 2 Key Features
 - ◆ 2.1 B200
 - ◆ 2.2 B210
 - ◆ 2.3 B200mini
 - ◆ 2.4 B200mini-i
 - ◆ 2.5 B205mini-i
- 3 Frontend Specifications
 - ◆ 3.1 Tuning
 - ◆ 3.2 Gains
 - ◆ 3.3 Bandwidths
- 4 RF Specifications
 - ◆ 4.1 RF Performance
 - ◆ 4.2 Input/Output Impedance
 - ◆ 4.3 Input Power Levels
 - ◆ 4.4 RF Performance Data
 - ◇ 4.4.1 B200mini / B205mini
 - ◇ 4.4.2 B200 / B210
- 5 Hardware Specifications
 - ◆ 5.1 B200
 - ◆ 5.2 B210
 - ◆ 5.3 B200mini
 - ◆ 5.4 B200mini-i
 - ◆ 5.5 B205mini-i
- 6 Physical Specifications
 - ◆ 6.1 Dimensions
 - ◆ 6.2 Weight
 - ◆ 6.3 Drawings
 - ◇ 6.3.1 B200mini
 - ◇ 6.3.2 B200
 - ◇ 6.3.3 B210
 - ◇ 6.3.4 B200/B210 Enclosure
 - ◆ 6.4 CAD/STP Models
 - ◇ 6.4.1 B200mini
 - ◇ 6.4.2 B20xmini-i
 - ◇ 6.4.3 B200
 - ◇ 6.4.4 B210
 - ◇ 6.4.5 B200/B210 Enclosure
- 7 Environmental Specifications
 - ◆ 7.1 Operating Temperature Range
 - ◆ 7.2 Operating Humidity Range
- 8 Schematics
 - ◆ 8.1 B200mini/B200mini-i/B205mini-i
 - ◆ 8.2 B200/B210
- 9 Key Component Datasheets
- 10 Enclosures
 - ◆ 10.1 B200mini
 - ◆ 10.2 B205mini
 - ◆ 10.3 B200/B210
- 11 FPGA
 - ◆ 11.1 B200
 - ◆ 11.2 B210
 - ◆ 11.3 B200mini
 - ◆ 11.4 B205mini
- 12 Interfaces and Connectivity
 - ◆ 12.1 GPIO
 - ◇ 12.1.1 Power on state
 - ◇ 12.1.2 Output Current
 - ◆ 12.2 Timing Reference Input
 - ◇ 12.2.1 B200mini/B200mini-i/B205mini-i
 - 12.2.1.1 1-PPS
 - 12.2.1.2 10 MHz
 - ◇ 12.2.2 B200/B210
 - 12.2.2.1 1-PPS
 - 12.2.2.2 10 MHz
- 13 Certifications
 - ◆ 13.1 RoHS
 - ◆ 13.2 China RoHS
 - ◆ 13.3 Certifications for European Union
- 14 Certificate of Volatility
- 15 Downloads
- 16 FAQ

The USRP Bus Series provides a fully integrated, single board, Universal Software Radio Peripheral platform with continuous frequency coverage from 70 MHz to 6 GHz. Designed for low-cost experimentation, it combines a fully integrated direct conversion transceiver providing up to 56MHz of real-time bandwidth, an open and reprogrammable Spartan6 FPGA, and fast and convenient bus-powered SuperSpeed USB 3.0 connectivity.

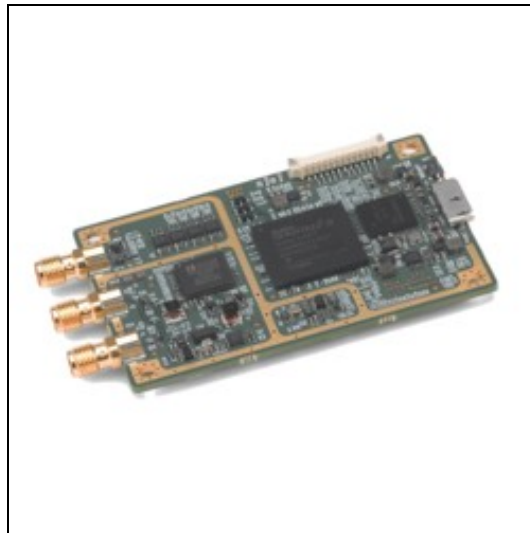
- Xilinx Spartan 6 XC6SLX75 FPGA
- Analog Devices AD9364 RFIC direct-conversion transceiver
- Frequency range: 70 MHz - 6 GHz
- Up to 56 MHz of instantaneous bandwidth
- Full duplex, SISO (1 Tx & 1 Rx)
- Fast and convenient bus-powered USB 3.0 connectivity
- Optional Board Mounted GPSDO



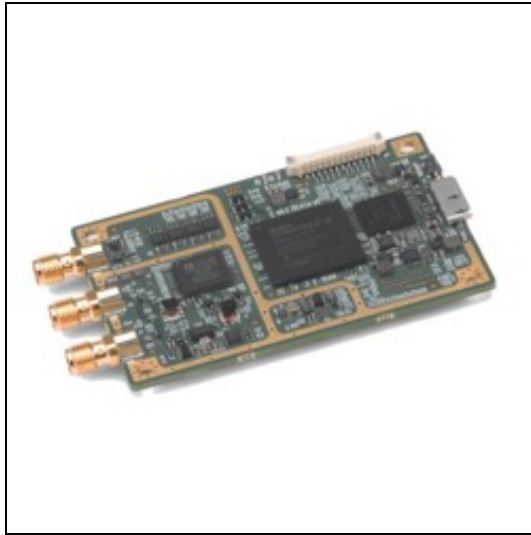
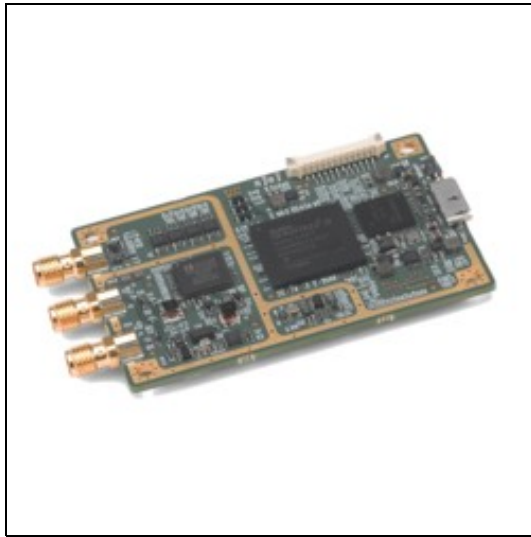
- Xilinx Spartan 6 XC6SLX150 FPGA
- Analog Devices AD9361 RFIC direct-conversion transceiver
- Frequency range: 70 MHz - 6 GHz
- Up to 56 MHz of instantaneous bandwidth (61.44MS/s quadrature)
- Full duplex, MIMO (2 Tx & 2 Rx)
- Fast and convenient bus-powered USB 3.0 connectivity
- Optional Board Mounted GPSDO



- Xilinx Spartan-6 XC6SLX75 FPGA
- Analog Devices AD9364 RFIC direct-conversion transceiver
- Frequency range: 70 MHz - 6 GHz
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- Full duplex, SISO (1 Tx & 1 Rx)
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- Industrial-grade Xilinx Spartan-6 XC6SLX75 FPGA
- Analog Devices AD9364 RFIC direct-conversion transceiver
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- Industrial-grade Xilinx Spartan-6 XC6SLX150 FPGA
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The RF frontend has individually tunable receive and transmit chains. On the B200 and B200 mini, there is one transmit and one receive RF frontend. On the B210, both transmit and receive can be used in a MIMO configuration. For the MIMO case on the B210 only, both receive frontends share the RX LO, and both transmit frontends share the TX LO. Each LO is independently tunable between 50 MHz and 6 GHz and can be used with 1 or 2 channels; all channels using the same LO must use the same sampling parameters, including the sample rate and RF center frequency.

All frontends have individual analog gain controls. The receive frontends have 76 dB of available gain; and the transmit frontends have 89.8 dB of available gain. Gain settings are application specific, but it is recommended that users consider using at least half of the available gain to get reasonable dynamic range.

The analog frontend has a seamlessly adjustable bandwidth of 200 kHz to 56 MHz.

Generally, when requesting any possible master clock rate, UHD will automatically configure the analog filters to avoid any aliasing (RX) or out-of-band emissions whilst letting through the cleanest possible signal.

If you, however, happen to have a very strong interferer within half the master clock rate of your RX LO frequency, you might want to reduce this analog bandwidth. You can do so by calling `uhd::usrp::multi_usrp::set_rx_bandwidth(bw)`.

The property to control the analog RX bandwidth is `bandwidth/value`.

UHD will not allow you to set bandwidths larger than your current master clock rate.

The USRP B200/B210/B200mini/B205mini are derived from the Analog devices AD936x integrated transceiver chip, the overall RF performance of the device is largely governed by the transceiver chip itself.

- SSB/LO Suppression -35/50 dBc
- Phase Noise 3.5 GHz 1.0 deg RMS
- Phase Noise 6 GHz 1.5 deg RMS
- Power Output >10dBm
- IIP3 (@ typ NF) -20dBm
- Typical Noise Figure <8dB
- Maximum Input Power: -15 dBm

All RF Ports are matched to 50 Ohm with -10dB or better return loss generally. Detailed test is pending.

- The maximum input power for the B200/B210/B200mini/B205mini is -15 dBm.

- [Media:B200mini B205 RF Performance Data 20160119.pdf](#)

- [Media:B200 RF Performance.pdf](#)

- Ettus Research recommends to always use the latest stable version of UHD

- Current Hardware Revision: 6
- Minimum version of UHD required: 3.8.4
- B200 Rev 5 (AD9364-based board) requires minimum UHD 3.8.4

- Current Hardware Revision: 5
- Minimum version of UHD required: 3.6.0

- Current Hardware Revision: 2
- Minimum version of UHD required: 3.9.0

- Current Hardware Revision: 2
- Minimum version of UHD required: 3.9.0

- Current Hardware Revision: 1
- Minimum version of UHD required: 3.9.2

- B200mini/B205mini 5.0 x 8.4 cm
- B200/B210 9.7 x 15.5 x 1.5 cm

- B200mini 24.0 g
- B200/B210 350 g

- [Board only](#)
- [B20xmini Enclosure](#)

- [Board only](#)

- [Board only](#)

- [Enclosure](#)

- [B200mini with Enclosure](#)
- [Enclosure only](#)
- [Board only](#)

- [B20xmini-i Thermal Insert](#)

- [Board only](#)

- [Board only](#)

- [Enclosure](#)

- B200 / B210: 25 °C
- B200mini - Board Only: 0 - 40 °C
- B200mini - With Enclosure: -20 - 60 °C
- B200mini-i / B205mini-i - Board Only: 0 - 45 °C
- B200mini-i / B205mini-i - With I-Grade Enclosure: -40 - 75 °C

- 10% to 90% non-condensing

B200/B210 Schematics

| Part Number | Description | Schematic ID (Page) |
|--------------------------------------|---------------------------------|--|
| Mini-Circuits TCM1-63AX+ | Transformer | T1 (1,3); T2 (1,3) |
| Analog Devices AD9364 | RF Transceiver | U1 (2) |
| Analog Devices AD9361 | RF Transceiver | U2 (2,8) |
| AD9361/AD9364 Product Page | RF Transceiver | - |
| Xilinx Spartan-6 Product Page | FPGA | U1 (2,3,4,6); PG1 (6); U18B, U18C (7); U18D (8); U18E, U18F (9); U18G, U18H (10) |
| XC6SLX75 / XC6SLX150 | FPGA | |
| ADF4001 | Frequency Synthesizer | U101 (1) |
| CYUSB3014 | FX3: SuperSpeed USB Controller | U3 (5,6); U13 (5) |
| EZ-USB FX3? Product Page | | |
| SKY13317 | Antenna Switch | U801, U810 (8) |
| BD3150L50100A00 | Balun | U802, U808, U809, U815 (8) |
| PGA?102+ | Amplifier | U804, U817 (8) |
| VCTCXO | VCTCXO (B200mini only) | - |
| 525L20DA40M0000 | VCTCXO (B200/B210 only) | X100 (1) |
| Jackson Labs LC_XO Spec Sheet Manual | Optional GPSDO (B200/B210 only) | U100 (1) |

- SMA connectors should be torqued to 4 inch-pounds

- B200mini C-Grade Enclosure
- B200mini I-Grade Enclosure

- B205mini I-Grade Enclosure

- USRP B200/B210 Enclosure
 - ◆ Full Steel Enclosure
 - ◆ Compatible with green USRP B200 and B210 devices (revision 6 or later)
 - ◆ Front and rear K-Slots for anti-theft protection

- Utilization statistics are subject to change between UHD releases. This information is current as of UHD 3.9.4.

Device utilization summary:

Selected Device : 6slx75fgg484-3

Slice Logic Utilization:

| | | | | |
|----------------------------|-------|--------|-------|-----|
| Number of Slice Registers: | 15781 | out of | 93296 | 16% |
| Number of Slice LUTs: | 19987 | out of | 46648 | 42% |
| Number used as Logic: | 15983 | out of | 46648 | 34% |
| Number used as Memory: | 4004 | out of | 11072 | 36% |
| Number used as RAM: | 972 | | | |
| Number used as SRL: | 3032 | | | |

Slice Logic Distribution:

| | | | | |
|-------------------------------------|-------|--------|-------|-----|
| Number of LUT Flip Flop pairs used: | 24062 | | | |
| Number with an unused Flip Flop: | 8281 | out of | 24062 | 34% |
| Number with an unused LUT: | 4075 | out of | 24062 | 16% |
| Number of fully used LUT-FF pairs: | 11706 | out of | 24062 | 48% |
| Number of unique control sets: | 434 | | | |

IO Utilization:

| | | | | |
|-------------------------|-----|--------|-----|-----|
| Number of IOs: | 172 | | | |
| Number of bonded IOBs: | 155 | out of | 280 | 55% |
| IOB Flip Flops/Latches: | 124 | | | |

Specific Feature Utilization:

| | | | | |
|------------------------------|-----|--------|-----|-----|
| Number of Block RAM/FIFO: | 144 | out of | 172 | 83% |
| Number using Block RAM only: | 144 | | | |
| Number of BUFG/BUFGCTRLs: | 4 | out of | 16 | 25% |
| Number of DSP48A1s: | 76 | out of | 132 | 57% |

Device utilization summary:

Selected Device : 6slx150fgg484-3

Slice Logic Utilization:

| | | | | |
|----------------------------|-------|--------|--------|-----|
| Number of Slice Registers: | 29310 | out of | 184304 | 15% |
| Number of Slice LUTs: | 36486 | out of | 92152 | 39% |
| Number used as Logic: | 29279 | out of | 92152 | 31% |
| Number used as Memory: | 7207 | out of | 21680 | 33% |
| Number used as RAM: | 1752 | | | |
| Number used as SRL: | 5455 | | | |

Slice Logic Distribution:

| | | | | |
|-------------------------------------|-------|--------|-------|-----|
| Number of LUT Flip Flop pairs used: | 43635 | | | |
| Number with an unused Flip Flop: | 14325 | out of | 43635 | 32% |

| | | | | |
|------------------------------------|-------|--------|-------|-----|
| Number with an unused LUT: | 7149 | out of | 43635 | 16% |
| Number of fully used LUT-FF pairs: | 22161 | out of | 43635 | 50% |
| Number of unique control sets: | 723 | | | |

IO Utilization:

| | | | | |
|-------------------------|-----|--------|-----|-----|
| Number of IOs: | 180 | | | |
| Number of bonded IOBs: | 163 | out of | 338 | 48% |
| IOB Flip Flops/Latches: | 148 | | | |

Specific Feature Utilization:

| | | | | |
|------------------------------|-----|--------|-----|-----|
| Number of Block RAM/FIFO: | 186 | out of | 268 | 69% |
| Number using Block RAM only: | 186 | | | |
| Number of BUFG/BUFGCTRLs: | 4 | out of | 16 | 25% |
| Number of DSP48A1s: | 152 | out of | 180 | 84% |

Device utilization summary:

Selected Device : 6slx75csg484-3

Slice Logic Utilization:

| | | | | |
|----------------------------|-------|--------|-------|-----|
| Number of Slice Registers: | 15949 | out of | 93296 | 17% |
| Number of Slice LUTs: | 19963 | out of | 46648 | 42% |
| Number used as Logic: | 16140 | out of | 46648 | 34% |
| Number used as Memory: | 3823 | out of | 11072 | 34% |
| Number used as RAM: | 972 | | | |
| Number used as SRL: | 2851 | | | |

Slice Logic Distribution:

| | | | | |
|-------------------------------------|-------|--------|-------|-----|
| Number of LUT Flip Flop pairs used: | 23859 | | | |
| Number with an unused Flip Flop: | 7910 | out of | 23859 | 33% |
| Number with an unused LUT: | 3896 | out of | 23859 | 16% |
| Number of fully used LUT-FF pairs: | 12053 | out of | 23859 | 50% |
| Number of unique control sets: | 429 | | | |

IO Utilization:

| | | | | |
|-------------------------|-----|--------|-----|-----|
| Number of IOs: | 123 | | | |
| Number of bonded IOBs: | 114 | out of | 328 | 34% |
| IOB Flip Flops/Latches: | 147 | | | |

Specific Feature Utilization:

| | | | | |
|------------------------------|-----|--------|-----|-----|
| Number of Block RAM/FIFO: | 110 | out of | 172 | 63% |
| Number using Block RAM only: | 110 | | | |
| Number of BUFG/BUFGCTRLs: | 6 | out of | 16 | 37% |
| Number of DSP48A1s: | 76 | out of | 132 | 57% |
| Number of PLL_ADVs: | 1 | out of | 6 | 16% |

Device utilization summary:

Selected Device : 6slx150csg484-3

Slice Logic Utilization:

| | | | | |
|----------------------------|-------|--------|--------|-----|
| Number of Slice Registers: | 15949 | out of | 184304 | 8% |
| Number of Slice LUTs: | 19963 | out of | 92152 | 21% |
| Number used as Logic: | 16140 | out of | 92152 | 17% |
| Number used as Memory: | 3823 | out of | 21680 | 17% |
| Number used as RAM: | 972 | | | |
| Number used as SRL: | 2851 | | | |

Slice Logic Distribution:

| | | | | |
|-------------------------------------|-------|--------|-------|-----|
| Number of LUT Flip Flop pairs used: | 23859 | | | |
| Number with an unused Flip Flop: | 7910 | out of | 23859 | 33% |
| Number with an unused LUT: | 3896 | out of | 23859 | 16% |
| Number of fully used LUT-FF pairs: | 12053 | out of | 23859 | 50% |
| Number of unique control sets: | 429 | | | |

IO Utilization:

| | | | | |
|-------------------------|-----|--------|-----|-----|
| Number of IOs: | 123 | | | |
| Number of bonded IOBs: | 114 | out of | 338 | 33% |
| IOB Flip Flops/Latches: | 147 | | | |

Specific Feature Utilization:

| | | | | |
|------------------------------|-----|--------|-----|-----|
| Number of Block RAM/FIFO: | 110 | out of | 268 | 41% |
| Number using Block RAM only: | 110 | | | |
| Number of BUFG/BUFGCTRLs: | 6 | out of | 16 | 37% |
| Number of DSP48A1s: | 76 | out of | 180 | 42% |
| Number of PLL_ADVs: | 1 | out of | 6 | 16% |

B200/B210/B200mini - USB 3.0

The hardware power on state and UHD initial state for the front-panel GPIOs is high-Z. For the B2xx, B2xxmini there are no external pull-ups/pull-downs for the GPIO pins, but the FPGAs do have them and they are configured as follows: B2xx: pull-up, B2xxmini: pull-up.

The GPIOs are configured as LVCMOS33 outputs with pull-ups on the B2xx. The strength for LVCMOS and LVTTTL on Spartan 6 is 12 mA if not otherwise specified.

- 1-PPS or 10 MHz input
- Maximum: -5V / +5V
- Minimum: 0V / +2.5V

- Maximum: 0V / +5V
- Minimum: 0V / +1.8V

OR

- +10dBm ~ +27dBm
- Maximum: 5V
- Maximum: 15dBm (3.5Vpp into 50 ohms)

As of December 1st, 2010 all Ettus Research products are RoHS compliant unless otherwise noted. More information can be found at <http://ettus.com/legal/rohs-information>

Management Methods for Controlling Pollution Caused by Electronic Information Products Regulation

Chinese Customers

National Instruments is in compliance with the Chinese policy on the Restriction of Hazardous Substances (RoHS) used in Electronic Information Products. For more information about the National Instruments China RoHS compliance, visit ni.com/environment/rohs_china.

In order to ensure compliance with EU certifications for radio equipment, a ferrite bead (included in kits with NI part number 785825-01 and 785826-01) should be affixed onto the GPIO cable, if in use. This is achieved by opening the snap-on ferrite bead and enclosing it around the GPIO cable(s).

In addition to the part numbers listed above, these ferrite beads can be sourced through Fair-Rite using part number 0443164251.

Found on the [NI Product Certifications lookup tool](#) here.

[FPGA Resources](#)

[UHD Stable Binaries](#)

[UHD Source Code on Github](#)

This is a list of frequently asked questions on the USRP [B200/B210/B200mini](#). If you have questions that are not answered in this document, please contact us - info@ettus.com.

Will the USRP B200/B210 work with USB 2.0?

Yes, both the USRP B200 and USRP B210 will fall back to the USB 2.0 standard if a USB 3.0 port is not available. There are several things to consider. First, the USB 2.0 data rates are slower. Depending on the USB controller, operating system, and other factors, you may achieve a sample rate up to 8 MS/s with USB 2.0. Also, you may not be able to bus-power the USRP B200/B210 in USB 2.0 mode.

What samples rates should I expect with USB 3.0? USB 2.0?

The performance and throughput of USB 3.0 can vary between host controllers. Ettus Research recommends using the Intel Series 7, 8, and 9 USB controllers. In Linux, the command `lspci` will show the USB controller on the system.

When can I power the USRP B200/B210/B200mini off USB?

The experience will vary across various controllers. Generally speaking, bus-power is ideal for SISO operation. If you are using both channels of a USRP B210 we recommend an external power supply. We [sell an external power supply that works with a variety of USRPs](#).

MIMO operation with the USRP B210 is not recommended when using the USRP B210 on bus-power. It is also not recommended to run the B210 on bus-power if a GPS-disciplined oscillator is installed.

How much power does the USRP consume?

The table below shows power consumption (Watts) of a USRP B210 run with a 6V power supply. Figures on a 5V supply (USB power), or with a USRP B200 will be moderately lower. The sample rates shown are aggregate sample rates on the USB 3.0 interface.

| | 5 Msps | 15.36 Msps | 30.72 Msps | 56 Msps | 61.44 Msps |
|-------------------|--------|------------|------------|---------|------------|
| 1 RX | 1.92 | 2.112 | 2.184 | 2.508 | |
| 2 RX | 2.148 | 2.436 | 2.508 | 2.64 | |
| 1 TX | 2.184 | 2.34 | 2.352 | 2.22 | |
| 2 TX | 2.76 | 2.88 | 2.904 | 2.64 | |
| Full Duplex (1x1) | 2.508 | 2.736 | 2.796 | 3.168 | |
| 2x2 MIMO | 3.252 | 3.588 | 3.672 | 4.11 | 4.092 |

Can I build a multi-unit system with the USRP B200/B210?

It is possible to synchronize multiple USRP B200/B210 devices using the 10 MHz/1 PPS inputs and an external distribution system like to the OctoClock-G. However, [USB 3.0/2.0 performance](#) varies dramatically when multiple devices are streaming through the same controller. Generally, we recommend using the USRP N200/N210 if you need to build a high-channel count system.

Can I access the source code for the USRP B200/B210?

Yes. The USRP B200/B210 is supported by the USRP Hardware Driver™ software. You can find the driver and FPGA source code for the USRP B200/B210, and all other USRP models, in the UHD git repository:

http://files.ettus.com/manual/page_build_guide.html

What operating systems does the USRP B200/B210 work on?

The USRP B200/B210 is supported on [Linux](#), [OSX \(MacOSX / macOS\)](#) and [Windows](#).

Does the USRP B200/B210 work with GNU Radio?

Yes. The USRP B200/B210 work with our GNU Radio plugin - [gr-uhd](#).

Does the USRP B200/B210 work with MATLAB and Simulink?

Yes. You need to install the [Communications System Toolbox Support Package for USRP Radio](#).

Does the USRP B200/B210 work with OpenBTS?

Yes. This is a third-party application and you can find instructions here: [OpenBTS - Build, Install, Run](#).

For support, please sign up and contact the [OpenBTS mailing list](#).

What tools do I need to program the FPGA?

The USRP [B200](#) and USRP [B210](#) include a Spartan 6 XC6SLX75 and XC6S150, respectively. The USRP B200 can be programmed with the free version of Xilinx tools, while the larger FPGA on the USRP B210 requires a licensed seat.

Can I use a GPSDO with the USRP B200/B210?

Ettus Research offers a [Board-Mounted GPS-Disciplined OCXO](#) and a [Board-Mounted GPS-Disciplined TCXO](#), which are compatible with the USRP B200/B210. These provide a high-accuracy XO, which can be disciplined to the global GPS standard. Please note: When the GPSDO OCXO model is integrated on the USRP B200/B210, the device should be powered with an external supply instead of USB bus power. The TCXO version can be USB bus powered.