X310 Device Recovery

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AN-305 by Nate Temple and Michael Dickens

This application note covers the process of recovering the USRP X300/X310 by flashing the FPGA image via the JTAG interface.

Note: This guide is written for Linux only. In theory it can be made to work on any OS that supports Xilinx Vivado.

For reference, please refer to the user manual page for the X300/X310.

- Host Computer
- USB2/3 port
- 1 GbE or 10 GbE network interface (NIC)
- Supports Xilinx Vivado Lab installation
- Supports UHD installation
- Connections from host to the X3x0 USRP via
- USB2 cable
- One of the following, depending on the host computer's NIC
 \$ SFP+ / RJ45 Adapter and Ethernet cable
 - - ♦ SFP+ DAC cable

This guide assumes you have a Linux-based host computer that supports Xilinx Vivado, with UHD installed into the default prefix /usr/local; for example we are using Ubuntu Linux and installed UHD from source using the default CMAKE_INSTALL_PREFIX. If you do not have UHD installed, please install it, for example via the Building and Installing the USRP Open-Source Toolchain (UHD and GNU Radio) on Linux Application Note.

We recommend using an X310 FPGA image provided by the host computer's UHD install, so that their versions match up. During runtime, UHD checks its version against that of all target USRPs' FPGA versions, and if they are too different then UHD prints an note about the mismatch and errors out.

There are circumstances where using different versions for the host UHD and FPGA image is necessary; performing this scenario is very similar to the steps in this guide, but requires some additional steps once the USRP is accessible via networking. We do not cover this scenario in this guide. If you need assistance under this scenario, please contact Ettus Support for assistance and we will provide you with the extra note steps.

If you do not have the FPGA images downloaded for your current host UHD install, you can obtain them by executing the command:

sudo uhd_images_downloader

Verify you have the FPGA images downloaded by running the command:

ls -alh /usr/local/share/uhd/images/usrp_x3*

```
user@host:~$ ls -alh /usr/local/share/uhd/images/usrp_x3*
                       1 root root 11M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x300_fpga_HG.bit
  rw-r
            - - r - - -
                      1 root root 15M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x300_fpga_HG.lvbitx

1 root root 11M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x300_fpga_XG.bit

1 root root 15M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x300_fpga_XG.lvbitx

1 root root 16M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x310_fpga_HG.bit

1 root root 21M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x310_fpga_HG.bit

1 root root 21M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x310_fpga_HG.lvbitx

1 root root 16M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x310_fpga_HG.lvbitx
                           root root 16M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x310_fpga_XG.bit
                       1
                            root root 21M Mar 17 00:37 /usr/local/share/uhd/images/usrp_x310_fpga_XG.lvbitx
 rw-r--r-- 1
user@host:~$
```

You will need to have an install of Xilinx Vivado Lab Edition, Xilinx Vivado Design Edition, or Xilinx Vivado System Edition. If you have none of those installed, then the minimum install is via Xilinx Vivado Lab Edition -- and that's what we cover in this guide. If you are using the Xilinx Vivado Design or System Edition then the paths may differ slightly from those described herein but the basic steps and process are the same; you can skip this section and go to the next one.

Xilinx Vivado Lab Edition can be downloaded from one the following links:

- current version
- legacy versions for older OSs

For this application note, we use an older Ubuntu and thus older Xilinx Vivado Lab Edition: 2015.4; we show Xilinx Vivado Lab Edition 2019.2 screenshots where they differ significantly from those in 2015.4. Regardless of the version of Xilinx Vivado you use, the steps below are roughly the same.



After the download is complete, you can verify the MD5 sum of the file if you choose to do so, since Xilinx provides a MD5 SUM Value for each download:

cd ~/Downloads

md5sum Xilinx_Vivado_Lab_Lin_2015.4_1118_2.tar.gz

Note: The filename and MD5 hash may differ from the screen capture shown. Verify the MD5 sum against the hash listed on the Xilinx download page.

```
user@host:~/Downloads$ md5sum Xilinx_Vivado_Lab_Lin_2015.4_1118_2.tar.gz
75bce66f7183d116bea864e536a9fb83 Xilinx_Vivado_Lab_Lin_2015.4_1118_2.tar.gz
user@host:~/Downloads$
```

Next, decompress the downloaded tarball:

tar -zxvf Xilinx_Vivado_Lab_Lin_2015.4_1118_2.tar.gz

Next, go into the new directory and run the xsetup installer using superuser sudo permissions:

cd Xilinx_Vivado_Lab_Lin_2015.4_1118_2 sudo ./xsetup

```
user@host:~/Downloads$ ls
Xilinx_Vivado_Lab_Lin_2015.4_1118_2 Xilinx_Vivado_Lab_Lin_2015.4_1118_2.tar.gz
user@host:~/Downloads$ cd Xilinx_Vivado_Lab_Lin_2015.4_1118_2/
```

```
user@host:~/Downloads/Xilinx_Vivado_Lab_Lin_2015.4_1118_2$ ls
bin data lib payload scripts tps xsetup
user@host:~/Downloads/Xilinx_Vivado_Lab_Lin_2015.4_1118_2$ sudo ./xsetup
```

This will launch the Xilinx Vivado Lab installer.



You might be prompted that a newer version is available; if so ignore this popup and click continue.

🛛 🖨 🕒 Vivado Lab	Edition 2015.4 Installer - Welcome
VIVADO.	Welcome
	We are glad you've chosen Xilinx as your platform development partner. This program can install the Vivado Lab Edition Environment.
	Supported operating systems for Vivado Lab Edition 2015.4 are: - Windows 7 SP1: 32 and 64-bit - Windows 8.1: 64-bit - Red Hat Enterprise Linux 6.5-6.6: 32 and 64-bit - Red Hat Enterprise Linux 7.0-7.1: 64-bit - CentOS Linux 7.1: 64-bit
	A Newer Version Is Available
	Xilinx Design Tools 2016.4 is now available. before continuing. Click Get Latest to download this latest version and cancel this installation. before continuing. Click Continue to continue with this installation of Xilinx design Tools 2015.4. before continuing.
E XILINX ALL PHOGRAMMABLE	
Copyright @ 1986-2017 Xiinx,	, Inc. All rights reserved. Preferences < Back Next > Cancel

The installer will then be at a Welcome screen, click ${\tt Next}.$



You will then be prompted to accept the various License Agreements, select all of the "I Agree" boxes then click Next.

😢 💿 💿 Vivado Lab Edition 2015.4 Installer - Accept License Agreements	
Accept License Agreements	
Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.	ALL PROGRAMMABLE.
 Xilinx Inc. End User License Agreement By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTW behalf of licensee to be bound by the agreement, which can be viewed by clicking here. ✓ I Agree WebTalk Terms And Conditions By checking "I AGREE" below, I also confirm that I have read Section 13 of the terms and conditions abo WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at http://www.xilinx.com understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of it to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 	VARE, YOU AGREE on we concerning om/webtalk, 1 they don't apply, 1 the internet. If I fail nformation, I agree n 13(b).
Third Party Software End User License Agreement By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTW behalf of licensee to be bound by the agreement, which can be viewed by <u>clicking here</u> .	VARE, YOU AGREE on
Copyright © 1986-2017 Xilinx, Inc. All rights reserved.	<u>N</u> ext > <u>C</u> ancel

You will then be prompted to select the install options. It is suggested to leave the default values, click Mext.

🍘 🗇 🗉 Vivado Lab Edition 2015.4 Installer - Vivado Lab Edition (Standalone)	
Vivado Lab Edition (Standalone)	
Customize your installation by (de)selecting items in the tree below. Moving cursor over selections below ALL PROGRAMMABLE.	
Installs only the Xilinx Vivado Lab Edition. This standalone product includes the Vivado Device Programmer and Vivado Logic Analyzer tools. Standalone Lab Edition is intended for use in lab environments where the full-featured Vivado Design Suite not required. Note: Device Programmer and Analyzer are also installed with all Vivado Design Editions and Vivado WebPACK products	
 P ★ Design Tools ✓ Vivado Lab P ✓ Installation Options NOTE: Cable Drivers are not installed on Linux. Please follow the instructions in UG973 to install Linux cable drivers ☑ NOTE: Cable Drivers are not installed on Linux. Please follow the instructions in UG973 to install Linux cable drivers ☑ Enable WebTalk to send usage statistics to Xilinx 	
<u>الا</u>	•
Download Size: NA Disk Space Required: 2.27 GB	
Copyright © 1986-2017 Xilinx, Inc. All rights reserved.	

You will then be prompted with the installation locations. The default value for older Xilinx Vivado Lab is /opt/Xilinx while for newer versions it is /tcols/Xilinx. We will be using the former here; what you use is your choice, but please note the install directory so that you can make sure to use it correctly later in this guide.

😕 🗇 💿 🛛 Vivado Lab Edition 201	.4 Installer - Select Destination Directory
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Select Destination Directory



Choose installation options such as location and shortcuts.

Installation Options Select the installation directory	Select shortcut and file association options		
/opt/Xilinx	Xilinx Design Tools		
Installation location(s) /opt/Xilinx/Vivado_Lab/2015.4	Create desktop shortcuts		
Disk Space Required			
Download Size: NA Disk Space Required: 2.27 GB Disk Space Available: 220.4 GB			
Copyright © 1986-2017 Xilinx, Inc. All rights reserved.	< <u>B</u> ack <u>N</u> ext > <u>C</u> ancel		

If the install directory does not exist, you will be prompted immediately to create it. Click ${\tt Yes.}$

🕲 🖨 🐵 Vivado Lab Edition 2015.4 Installer - Select Destin	nation Directory
Select Destination Directory	
Choose installation options such as location and shortcuts.	
Installation Options Select the installation directory	Select shortcut and file association options
/opt/Xilinx	Xilinx Design Tools
Installation location(s) /opt/Xilinx/Vivado_Lab/2015.4	Create <u>d</u> esktop shortcuts
Disk Space Required Disk Space Required: 2.27 G Disk Space Available: 220.4 ? /opt/Xilinx does not exist.	opt/Xilinx does not exis . do you want to create it? No
Copyright © 1986-2017 Xilinx, Inc. All rights reserved.	< <u>B</u> ack <u>N</u> ext > <u>C</u> ancel

Finally, you will be at the Installation Summary prompt. Click $\tt Install$.



The installer has to download files from the internet, but they are not large and hence the installation process typically takes only a few minute.

😕 🗇 🔍 Vivado Lab Edition 2015.4 Install	er - Installation Progress
Installation Progress	
Installing files, 35% completed.	
Final Processing	All Programmable
	Image: State of the state
	www.xilinx.com/apa
Copyright © 1986-2017 Xilinx, Inc. All rights reserved.	< <u>B</u> ack I <u>n</u> stall <u>C</u> ancel

You will then be prompted that the installation was successful. Click ${\scriptstyle \textsc{ok}},$ and the installer will close.



In order to use the JTAG interface built into the USRP X300/X310 front panel, you will need to install the Digilent Cable Driver. It is included with the Xilinx Vivado Lab Edition package.

Navigate to the folder /opt/Xilinx/Vivado_Lab/2015.4/data/xicom/cable_drivers/lin64/install_script/install_drivers, and run the installer script.

cd /opt/Xilinx/Vivado_Lab/2015.4/data/xicom/cable_drivers/lin64/install_script/install_drivers
sudo ./install_digilent.sh

usar@hast./ant/Xiliax/Vivada Lab/2015 4/data/vicam/cable drivers/lin64/install script/install drivers 1s .alb
total 28K
deux-vr-v 2 root root 4 AK Mar 17 AA+18
drugs rest a cost root 4 AK Mar 17 AR-18
- W
- we we we we have a start of the start and the start of
-rus-st-s 1 root root 1 9K Nov 17 2015 instatul drivers
- HWY-N-X 1 FOOT FOOT 2 AK NOV 17 2015 Statute provide
user@hast:/ant/%iliav/vivada_Lab/2015_4/data/vicom/cable_drivers/lin64/install_script/install_driversS_sudo_/install_dioilent_sh
Surgessfully installed Diollent Cable Drivers
user@hast:/only/livada_lab/2015_4/data/vicom/cable_drivers/lin64/install_script/install_drivers5

Next, reload the UDEV rules

sudo udevadm control --reload

You will need to set your ethernet interface that will be connected to the USRP X300/X310 to a static IP address of 192.168.10.1 along with setting a MTU of 1500.

Attach the SFP+/RJ45 adapter to Port 0 and connect your computer via ethernet.

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Ethernet Ne	twork		
Wired conn	ection 1		
Disconnect			
Wi-Fi Netwo Wi-Fi is disa	orks bled		
VPN Conne	ctions	>	
✓ Enable Netw Enable Wi-F	vorking i		
Connection	Information		
Edit Connec	tions		
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Connection name:	/ired connection 1		
General Ethernet	802.1x Security DCB	IPv4 Settings	IPv6 Settings
Method: Manual			•
Addresses			
Address	Netmask	Gateway	Add
192.168.10.1	255.255.255.0		Delete
DNS servers:	1		
Search domains:			
DHCP client ID:			
Require IPv4 ad	dressing for this con	nection to comp	lete
			Routes
			Cancel Save
		L	

Connect the host computer where Xilinx Vivado was installed to the USRP X300/X310 via a USB2 cable. On the USRP X300/X310, plug the USB2 cable into the JTAG port on the front face plate. Once the USB cable is connected on both sides, power on the USRP X300/X310.



Start by navigating back to your home directory:

cd ~/

Next, start Xilinx Vivado Lab via the commandline

/opt/Xilinx/Vivado_Lab/2015.4/bin/vivado_lab



This will bring up the main Vivado Lab window:

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VIVADO. Lab Edition	с. Е.
Quick Start	
Create New Project Open Project Open Hardware Manager	
Information Center	
Documentation and Tutorials	
Tcl Console	

The main window for more recent Xilinx Vivado Lab versions -- here 2019.2 -- will look slightly different:

Vivado Lab Edition 2019.2	🙁
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VIVADO. Lab Edition	E XILINX.
Quick Start Create Project >	
Open Project > Open Hardware Manager >	
Learning Center	
Documentation and Tutorials > Quick Take Videos > Release Notes Guide >	
Tcl Console	

Open the Hardware Manager by selecting Open Hardware Manager :

🥝 🗇 🕘 Vivado Lab Edition 2015.4	
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Quick Start	
Create New Project Open Project Open H	rdware Manager
Information Center	
Documentation and Tutorials Ouick Take Videos Relea	wide Suide
I Tcl Console	
Open the Hardware Manager to connect to a target JTAG cable or board. T	ils allows you to program devices, debug your design in-system, etc.

Vivado Lab Edition 2019.2	🙁
Eile Tools Window Help Q-Quick Access	
VIVADO. Lab Edition	E XILINX.
Quick Start Create Project > Open Project > Open Hardware Manager >	
Learning Center Documentation and Tutorials > Quick Take Videos > Release Notes Guide >	
Tcl Console	

This will enable a new window:

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No hardware target is open. Open target	
Hardware _ C X	
No content	
Properties _ D 12 X	
Select an object to see properties	
Tcl Console	- D & ×
start_gui open_hv	4
	¥ }
Type a Tcl command here	Intelligence
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	Vivado Lab Edition 2019.2	$\overline{\tau}$	•	8
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O No hardware target is open. Open target				
Hardware ? _ 🗆 🛙	×			
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No content				
No concent				
Properties ? _ 0	×			
+ +				
Select an object to see properties				
Td Console x Messages Serial I/O Li	s Serial I/O Scans	? .		3
Q				
start_gui open_hw_manager < Type a Tcl command here			,	

Next, within the menu the of the Hardware Manager select Tools -> Auto Connect.



The details of the FPGA should populate the window on the left side of the Hardware Manager.

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Elle Edit Tools Window Layout View Help Q- Search commands		
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There are no debug cores. Program device Refresh device		
Hardware		
Properties _ □ ℓ × ← → k Select an object to see properties		
Tcl Console	D Le X	
<pre>INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/25163500DC9EA current_hw_device [lindex [get_hw_devices] 0] INFO: [Labtools 27-1434] Device xc7k410t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it. WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3. Resolution: I. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR C. Manually launch hw_server with -e "set xsdb-user-bscan <c_user_scan_chain scan_chain_number="">" to detect the debug hub at User Scan (Interval) </c_user_scan_chain></pre>		
	•	
Type a Tcl command here		
🗏 Tcl Console 🕒 Messages 🐁 Serial VO Links 🔯 Serial VO Scans		

Right click on the FPGA listed, and select Program Device.

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There are no debug cores. Program device Refresh device		
Hardware _ C & X		
Name Status		
Iocalhost (1) Connected Connected		
Q-Q xC7k		
L W XA Ardware Device Properties Ctri+E		
Program Device		
Retresh Device		
Boot from Configuration Memory Device		
Program BBR Key		
Clear BBR Key		
Program eFUSE Registers		
Export to Spreadsheet		
Name: xc7k410t_0		
Part: xc7k410t		
ID code: 13656093		
IR length: 6		
General Properties		
Tcl Console _ D C	ĸ	
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/2516350DDC9EA	3	
Current_hw_device (lindex [get_hw_devices] 0]		
INFO: [Labtools 27-1434] Device xc7k410t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.		
WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3. Resolution:		
1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR		
1 D2. Manually launch hw_server with -e "set xsdb-user-bscan <c_user_scan_chain scan_chain_number="">" to detect the debug hub at User Scan</c_user_scan_chain>		
	-	
Type a Tcl command here	4	
😑 Tcl Console 💿 Messages 🗞 Serial I/O Links 📴 Serial I/O Scans		
Program hardware device with specified bitstream		

This will popup a new window. Click on the file selection button and navigate to the location of the UHD FPGA images, and select the correct FPGA image for your device. (/usr/local/share/uhd/images)

Note: Select the correct FPGA image that matches your USRP (either _x300 or _x310) with the .bit file extension. It is recommended to select the _Hg FPGA image, which will initialize Port 0 as 1 GbE and Port 1 as 10 GbE. Advanced users operating with dual 10 GbE may select the _xg image, however you will need to adjust the instructions listed within this document to match the dual 10GbE configuration (IP Addresses, MTU settings, etc).

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There are no debug cores.	Program device Befresh device	
Hardware		
<		
Name Norne	Connected	
	350DDC9EA (1) Open	
La XADC (System Mon	tor)	
	Program Device	
S	select a bitstream programming file and download it to your hardware device.	You can
Hardware Device Properties	itstream programming file.	
S κc7k410t 0	Photoso file	
	Bitstream hie:	
Part: xc7k410	Debug probes file:	Specify Bitstream file
ID code: 136560	Enable end of startup check	
IR length: 6		
٩ · · · · · · · · · · · · · · · · · · ·		
General Properties		
Tcl Console		- 0 2 ×
CINFO: [Labtoolstcl 4	ELOG	ram Cancer
Prefresh hw device -upd INFO: [Labtools 27-143]	ate hy probes false [lindex [get_hy_devices] 0] 41 Device xc7k410t (JTAG device index = 0) is programmed with a desig	n that has no supported debug core(s) in it.
WARNING: [Labtools 27-	3123] The debug hub core was not detected at User Scan Chain 1 or 3.	
1. Make sure the clock	connected to the debug hub (dbg_hub) core is a free running clock an	d is active OR
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Tcl Console OMessag	jes % Serial I/O Links 📓 Serial I/O Scans	
Program hardware device with s	pecified bitstream	
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Look jn images bit winusb_driver usrp_2.fpga.bin usrp_b100_fpga.bin usrp_b200_fpga.bin usrp_b200_mpga.bin usrp_b200_mpga.bin usrp_b210_fpga.bin usrp_b210_fpga.bin usrp_colo_fpga.bin usrp_colo_fpga.bin usrp_colo_fpga.bit usrp_e100_fpga.bit usrp_e100_fpga.bit usrp_e100_fpga.bit usrp_c000_fcga.bit	Recent Directories Recent Directories Recent Directories Recent Construction Recent Const
usrp_n2to_r_t_pga.bin usrp_r_t_pga.bin	
Files of type: [Bitstream Files (.bit, bin, rbt)	•
Specify Bitstream File	• # \$ #@A #X\$
bit 100 toga X0.bit	Recent Directories
usrp_sto_pga_bin usrp_sto_pga_X0.bt	a /home/user *
utrp2_hwbm utrp_b100_fpga_2ncbin utrp_b200_fnga_bin utrp_b200smin_fpga_bin utrp_b200smin_fpga_bin utrp_c80c_fpga_des_bt utrp_c80c_fpga_des_bt utrp_c80c_fpga_bn utrp_c110_fpga_bn utrp_c310_fpga_bt utrp_c310_fpga_bt utrp_c300_r2_fpga_bn utrp_c300_r2_fpga_bn utrp_c310_fwbh utrp_c300_r2_fpga_bn utrp_c310_fwbh utrp_c300_r4_fpga_bn utrp_c310_fwbh utrp_c300_r4_fpga_bn utrp_c310_fwbh	File Preview File: usrp_x10 (pga_H6.bt Directory: Just/local/sharpUnd/mages Created: Today at 00:37 AM Accessed: Today at 00:37 AM Size: 15.1 MB Type: Elistream file Owner: not Permissions: ner-r-
File game: Usrp_x310_fpga_H3 bit	
File pame: Uszp_x310_fpga_HG.bit Files of type: Btstream Files (.bit. bin. rbt)	
File pane: usrp_x310_fpga_HG.bit Files of type: Btstream Files (.bit, bin, rbt)	• CK Cancel

Next, click Program.



A progress bar will popup as the FPGA is programmed.

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There are no debug cores. Program device Refresh device		
Hardware _ D & X		
Name Status		
Connected Connected Connected		
Q = Q xc7k410t 0 (1) Programmed		
Le XADC (System Monitor)		
Hardware Device Properties _ D & ×		
Norma Program Device		
Name: xc7k41 W Commencies the device		
D code: 136560 Cancel		
IR length: 6		
Background		
General Properties		
Tcl Console _	. 🗆 🕹 ×	
INFO: [Labtools 27-1434] Device xc7k410t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it. WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3. Resolution: 1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR 2. Manually launch hw_server with -e "set xsdb-user-bscan <c_user_scan_chain scan_chain_number="">" to detect the debug hub at User Scan (set_property PROBES.FILE {} [lindex [get_hw_devices] 0] set_property PROGRAM.FILE {/usr/local/share/uhd/images/usrp_x310_fpga_HG.bit} [lindex [get_hw_devices] 0] program_hw_devices [lindex [get_hw_devices] 0]</c_user_scan_chain>		
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Type a Tcl command here		
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Programming the device	14	

Once the programming is completed, close Vivado Lab.

Note:: If Vivado is actively attached to the USRP (auto-connect is enabled for the specific target), then at USRP power cycle Vivado will stop the USRP from auto-loading whatever FPGA image is stored on it. If you are going to leave Vivado open, then make sure Vivado's session to the USRP is closed during the USRP power cycle to get the USRP to load the onboard FPGA image as usual. The USRP should boot fully and as usual so long as Vivado's session to it is closed, regardless of whether USB is plugged it (active or not) or if Vivado is running (so long as the session to the USRP target is not active).

🤒 🚍 🐵 Vivado Lab Edition 2015.4		
Eile Edit Tools Window Layout View Help	Q+ Search commands	
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There are no debug cores. Broorem device. Refrech device		
W mere are no debug cores. Program device Refear device		
Hardware _ C Z X		
©- I localhost (1) Connected		
∲- ø xilinx_tcf/Digilent/2516350DDC9EA (1) Open		
ADC (System Monitor)		
Hardving Davis Properties		
* KE/K4IULO		
Name: xc7k410t_0		
Part: xc7k410t		
ID code: 13656093		
IR length: 6		
General Properties		
Tri Console		
INFO: [Labtools 27-3164] End of startup status: HIGH		
program_hw_devices: Time (s): cpu = 00:00:10 ; elapsed	= 00:00:09 . Memory (MB): peak = 5519.723 ; gain = 0.000 ; free physical = 1295	
TNEO: [Labtools 27.1434] Device xc7k410t (ITAG device)	index = 0 is programmed with a design that has no supported debug core(s) in it	
WARNING: [Labtools 27-3123] The debug hub core was not	detected at User Scan Chain 1 or 3.	
Resolution:	hub) care is a free running clack and is active OR	
Annually launch hw_server with -e "set xsdb-user-bs	can <c_user_scan_chain scan_chain_number="">" to detect the debug hub at User Scan (</c_user_scan_chain>	
	V	
Type a Tcl command here		
🗏 Tcl Console 💿 Messages 🐁 Serial I/O Links 📴 Serial I/O Scans		

Return to a terminal and attempt to ping the USRP X300/X310.

ping 192.168.10.2

😣 🗐 🗊 user@host: ~

user@host:~\$ ping 192.168.10.2 PING 192.168.10.2 (192.168.10.2) 56(84) bytes of data. 64 bytes from 192.168.10.2: icmp_seq=1 ttl=32 time=1.03 ms 64 bytes from 192.168.10.2: icmp_seq=2 ttl=32 time=0.767 ms 64 bytes from 192.168.10.2: icmp_seq=3 ttl=32 time=0.778 ms 64 bytes from 192.168.10.2: icmp_seq=4 ttl=32 time=0.871 ms

Stop the ping with CTRL-C.

At this point, if you're able to ping the USRP X300/X310, attempt to run the UHD utility uhd_usrp_probe.

uhd_usrp_probe

Example output from uhd_usrp_probe:

Device: X-Series Device

user@host:~\$ uhd_usrp_probe linux; GNU C++ version 5.4.0 20160609; Boost_105800; UHD_003.010.001.HEAD-0-gc705922a

```
X300 initialization sequence...
Determining maximum frame size... 1472 bytes.
Setup basic communication...
Loading values from EEPROM...
Radio 1x clock:200
[DMA FIFO] Running BIST for FIFO 0... pass (Throughput: 1304.3MB/s)
[DMA FIFO] Running BIST for FIFO 1... pass (Throughput: 1300.5MB/s)
[RFNoC Radio] Performing register loopback test... pass
Performing timer loopback test... pass
Performing timer loopback test... pass
```

/ Mboard: X310
revision: 8
revision_compat: 7
product: 30818
mac-addr0: 00:00:00:00:00:00
mac-addr1: 00:00:00:00
gateway: 192.168.10.1
ip-addr0: 192.168.10.2
subnet0: 255.255.255.0
ip-addr1: 192.168.20.2
subnet1: 255.255.255.0
ip-addr2: 192.168.40.2
subnet3: 255.255.0
ip-addr3: 192.168.40.2
subnet3: 255.255.0
serial: xxxxxxx
FW Version: 5.1
FPGA Version: 33.0
RFNoC capable: Yes
Time sources: internal, external, gpsdo
Clock sources: internal, external, gpsdo
Sensors: ref_locked
//
RX Dboard: A
| ID: UBX-160 v1 (0x007a)
| Serial: xxxxxxx

RX Frontend: 0 Name: UBX RX Malle: USA KA Antennas: TX/RX, RX2, CAL Sensors: lo_locked Freq range: 10.000 to 6000.000 MHz Gain range PGA0: 0.0 to 31.5 step 0.5 dB Bandwidth range: 160000000.0 to 160000000.0 step 0.0 Hz Connection Type: IQ Uses LO offset: No RX Codec: A Name: ads62p48 Gain range digital: 0.0 to 6.0 step 0.5 dB RX Dboard: B RX Frontend: 0 Name: Unknown (Oxffff) - 0 Antennas: Sensors: Freq range: 0.000 to 0.000 MHz Gain Elements: None Bandwidth range: 0.0 to 0.0 step 0.0 Hz Connection Type: IQ Uses LO offset: No RX Codec: B Name: ads62p48 Gain range digital: 0.0 to 6.0 step 0.5 dB TX Dboard: A ID: UBX-160 v1 (0x0079) Serial: xxxxxxx TX Frontend: 0 Name: UBX TX Antennas: TX/RX, CAL Sensors: lo_locked Freq range: 10.000 to 6000.000 MHz Gain range PGA0: 0.0 to 31.5 step 0.5 dB Bandwidth range: 160000000.0 to 160000000.0 step 0.0 Hz Connection Type: QI Uses LO offset: No TX Codec: A Name: ad9146 Gain Elements: None TX Dboard: B TX Frontend: 0 Name: Unknown (Oxfff) - 0 Antennas: Sensors: Freq range: 0.000 to 0.000 MHz Gain Elements: None Bandwidth range: 0.0 to 0.0 step 0.0 Hz Connection Type: IQ Uses LO offset: No TX Codec: B Name: ad9146 Gain Elements: None RFNoC blocks on this device: DmaFIFO_0 Radio_0 Radio_1 * * DDC_0 DDC_1 * DUC 0 ÷ DUC_1

If running uhd_usrp_probe is successful, proceed with flashing the FPGA image with the UHD utility uhd_image_loader.

Note: Flashing the FPGA image via JTAG only does not write the FPGA image to EEPROM, you must run the uhd_image_loader to write the FPGA image to the internal EEPROM.

uhd_image_loader --args "type=x300,addr=192.168.10.2,fpga=HG"


```
user@host:~$ uhd_image_loader --args "type=x300,addr=192.168.10.2,fpga=HG"
linux; GNU C++ version 5.4.0 20160609; Boost_105800; UHD_003.010.001.HEAD-0-gc705922a
Unit: USRP X310 (30DDC9E, 192.168.10.2)
FPGA Image: /usr/local/share/uhd/images/usrp_x310_fpga_HG.bit
-- Initializing FPGA loading...successful.
-- Loading HG FPGA image: 100% (121/121 sectors)
-- Finalizing image load...successful.
Power-cycle the USRP X310 to use the new image.
user@host:~$
```

Power off the USRP X300/X310, remove the JTAG USB cable, and then power on the USRP X300/X310.

The USRP X300/X310 is now recovered. You should be able to ping, run uhd_usrp_probe and any other UHD utility/application as normal.