# N210

## Contents



The USRP Network Series offers high-bandwidth, high-dynamic range processing capability. The Gigabit Ethernet interface of the USRP Network Series allows high-speed streaming capability up to 50 MS/s in both directions (8-bit samples). These features, combined with plug-and-play MIMO capability make the USRP Network an ideal candidate for software defined radio systems with demanding performance requirements.

- 50 MHz of RF bandwidth with 8 bit samples
- 25 MHz of RF bandwidth with 16 bit samples
- Gigabit Ethernet connectivity
- MIMO capable - requires two or more USRP N200 devices as motherboard has one daughterboard slot (1 RX + 1 TX connectors)
- Onboard FPGA processing
- FPGA: Xilinx® Spartan® 3A-DSP XC3SD1800A
- ADCs: 14-bits 100 MS/s
- DACs: 16-bits 400 MS/s
- Ability to lock to external 5 or 10 MHz clock reference
- TCXO Frequency Reference (~2.5ppm)
- Optional internal GPS locked reference oscillator
- FPGA code can be changed with Xilinx® ISE® WebPACK? tools
- Frequency range: DC - 6 GHz with suitable daughterboard

- 50 MHz of RF bandwidth with 8 bit samples
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- Onboard FPGA processing
- FPGA: Xilinx® Spartan® 3A-DSP XC3SD3400A
- ADCs: 14-bits 100 MS/s
- DACs: 16-bits 400 MS/s
- Ability to lock to external 5 or 10 MHz clock reference
- TCXO Frequency Reference (~2.5ppm)
- Optional internal GPS locked reference oscillator
- FPGA code can only be changed with the paid version of the Xilinx® ISE® Design Suite tools
- Frequency range: DC - 6 GHz with suitable daughterboard

- SBX-40
- UBX-40
- WBX-40
- CBX-40

- LFRX / LFTX
- BasicRX / BasicTX
- DBSRX2 (EOL)
- RFX Series (EOL)
- TVRX2 (EOL)

- SSB/LO Suppression -35/50 dBc
- Phase Noise 1.8 GHz 10kHz -80 dBc/Hz
- Phase Noise 1.8 GHz 100kHz -100 dBc/Hz
- Phase Noise 1.8 GHz 1MHz -137 dBc/Hz
- Power Output 15 dBm
- IIP3 (@ typ NF) 0 dBm
- Typical Noise Figure 5 dB

- Ettus Research recommends to always use the latest stable version of UHD

- Current Hardware Revision: 4
- Minimum version of UHD required: 3.8.0

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22 x 16 x 5 cm

1.2 kg

- File:cu usrp-n2x0 motherboard.pdf
- File:cu ettus-usrp-n2x0.pdf

- Motherboard

- Enclosure

- N200/N210: 25 °C

- 10% to 90% non-condensing

N200/N210 Schematics

| Part Number | Description | Schematic ID (Page) |
|---|---|---|
| AD9777 | Dual Channel, 16-Bit DAC | U3 (1) |
| ADS62P4X | Dual Channel, 14-Bit ADC | U2 (1) |
| XC3SD3400AFG676 | FPGA | U1 (2,8,9,10,11,12) |
| AD9510 | Clock Distribution IC | U9 (4) |
| ET1011C2 | Gigabit Ethernet Transceiver | U12 (6) |
| CY7C1354C | Pipelined SRAM | U19 (7) |
| MAX232 | Drivers/Receiver | U25 (10) |

- Utilization statistics are subject to change between UHD releases. This information is current as of UHD 3.9.4 and was taken directly from Xilinx Vivado 2014.4.

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Device utilization summary:
---------------------------

Selected Device : 3sd1800afg676-5

 Number of Slices:                    18356  out of  16640   110% (*)
 Number of Slice Flip Flops:          20466  out of  33280    61%
 Number of 4 input LUTs:              32968  out of  33280    99%
    Number used as logic:             28511
    Number used as Shift registers:    3945
    Number used as RAMs:                512
 Number of IOs:                         338
 Number of bonded IOBs:                 331  out of    519    63%
    IOB Flip Flops:                     342
 Number of BRAMs:                        41  out of     84    48%
 Number of GCLKs:                         6  out of     24    25%
 Number of DCMs:                          1  out of      8    12%
 Number of DSP48s:                       31  out of     84    36%
```

```
Device utilization summary:
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Selected Device : 3sd3400afg676-5

 Number of Slices:                    18349  out of  23872    76%
 Number of Slice Flip Flops:          20475  out of  47744    42%
 Number of 4 input LUTs:              32986  out of  47744    69%
    Number used as logic:             28529
    Number used as Shift registers:    3945
    Number used as RAMs:                512
 Number of IOs:                         338
 Number of bonded IOBs:                 331  out of    469    70%
    IOB Flip Flops:                     342
 Number of BRAMs:                        41  out of    126    32%
 Number of GCLKs:                         6  out of     24    25%
 Number of DCMs:                          1  out of      8    12%
 Number of DSP48s:                       31  out of    126    24%
```

- Gigabit Ethernet

As of December 1st, 2010 all Ettus Research products are RoHS compliant unless otherwise noted. More information can be found at http://ettus.com/legal/rohs-information

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**Chinese Customers**

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- Media:volatility USRP N200 N210 r2.pdf

For a detailed guide to recovering the N200/N210, please see the N200/N210 Device Recovery application note.

FPGA Resources

UHD Stable Binaries

UHD Source Code on Github