N321

Contents

The USRP N320 is a networked software defined radio that provides reliability and fault-tolerance for deployment in large scale and distributed wireless systems. This is a high performance SDR that uses a unique RF design by Ettus Research to provide 2 RX and 2 TX channels in a half-wide RU form factor. Each channel provides up to 200 MHz of instantaneous bandwidth, and covers a frequency range from 3 MHz to 6 GHz. The baseband processor uses the Xilinx Zynq-7100 SoC to deliver a large user programmable FPGA for real-time, low latency processing and a dual-core ARM CPU for stand-alone operation.Support for 1 GbE, 10 GbE, and Aurora interfaces over two SPF+ ports and 1 QSFP+ port enables high throughput IQ streaming to a host PC or FPGA coprocessor. A flexible synchronization architecture with support for LO sharing for TX and RX, 10 MHz clock reference, PPS time reference, GPSDO, and White Rabbit enables implementation of phase coherent MIMO testbeds. The USRP N320 leverages recent software developments in UHD to simplify control and management of multiple devices over the network with the unique capability to remotely administrate tasks such as debugging, updating software, rebooting, resetting to factory state, and monitoring system health.

- Xilinx Zynq-7100 FPGA SoC
- Dual-core ARM A9 800 MHz CPU
- 2 RX, 2 TX in half-wide RU form factor
- 3 MHz ? 6 GHz frequency range
- Up to 200 MHz of instantaneous bandwidth per channel
- Sub-octave RX, TX filter bank
- 14 bit ADC, 16 bit DAC

- Configurable sample rates: 200, 245.76, 250 MS/s
- Two SFP+ ports (1 GbE, 10 GbE, Aurora, White Rabbit)
- One QSFP+ port (2x 10Gb / Aurora)
- RJ45 (1 GbE)
- 10 MHz clock reference
- PPS time reference
- External RX, TX LO input ports
- Built-in GPSDO
- 1 Type A USB host port
- 1 micro-USB port (serial console, JTAG)
- Trusted Platform Module (TPM) v1.2
- Watchdog timer
- OpenEmbedded Linux
- Reliable and fault-tolerant deployment
- Remote management capability
- Stand-alone operation

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- RJ45 (1 GbE)
- 10 MHz clock reference
- PPS time reference
- External RX, TX LO input ports
- LO Distribution for up to 128x128 MIMO
- Built-in GPSDO
- 1 Type A USB host port
- 1 micro-USB port (serial console, JTAG)
- Trusted Platform Module (TPM) v1.2
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- Number of channels: 2
- Frequency Range: 3 MHz to 6 GHz
- Maximum instantaneous bandwidth: 200 MHz

- Maximum output power (P? out?): See Table 1
- Gain range
  - 0 dB to 60 dB (1 MHz to 6 GHz)

- Gain step: 1 dB
- Supported I/Q sample rates:
  - 200 MHz, 245.76 MHz, 250 MHz

- Output third-order intercept (OIP3) See Table 2

- Tuning Time: 245 us

- TX/RX Switching Time: 750 ns

- Filter Banks
  - 450 ? 650 MHz
  - 650 ? 1000 MHz
  - 1000 ? 1350 MHz
  - 1350 ? 1900 MHz

- ♦ 1900 ? 3000 MHz
- ♦ 3000 ? 4100 MHz
- ♦ 4100 ? 6000 MHz

- External LO Frequency Range: 450 MHz - 6.0 GHz

Frequency	Maximum Output Power
3 MHz - 450 MHz	+10 dBm
450 MHz - 1000 MHz	+20 dBm
1 GHz - 4.25 GHz	+18 dBm
4.25 GHz - 6 GHz	+15 dBm

Table 1: Maximum Output Power

Frequency	Output Third-Order Intercept (OIP3)
3 MHz - 450 MHz	> 15 dBm
450 MHz - 1.6 GHz	> 28 dBm
1.6 GHz - 5.8 GHz	> 25 dBm
5.8 GHz - 6.0 GHz	> 23 dBm

Table 2: Output Third-Order Intercept (OIP3)

Frequency Offset	1.0 GHz	2.0 GHz	3.0 GHz	5.5 GHz
10 kHz	-117	-110	-108	-103
100 kHz	-117	-110	-108	-104
1 MHz	-145	-137	-135	-130

Table 3: TX Phase Noise (dBc/Hz)

- Number of channels: 2
- Frequency Range: 3 MHz to 6 GHz
- Maximum instantaneous bandwidth: 200 MHz
- Gain range
  - ♦ 0 dB to 60 dB (1 MHz to 6 GHz)
- Gain step: 1 dB
- Maximum recommended input power (P? in?) 1 dB: -15 dBm

- Noise figure: See Table 3

- Third-order intermodulation distortion (IMD3) See Table 4

- Supported I/Q sample rates
  - ♦ 200 MHz, 245.76 MHz, 250 MHz

- Tuning Time: 245 us

- TX/RX Switching Time: 750 ns

- Filter Banks
  - ♦ 450 ? 760 MHz
  - ♦ 760 ? 1100 MHz
  - ♦ 1100 ? 1410 MHz
  - ♦ 1410 ? 2050 MHz
  - ♦ 2050? 3000 MHz
  - ♦ 3000 ? 4500 MHz
  - ♦ 4500 ? 6000 MHz

- External LO Frequency Range: 450 MHz - 6.0 GHz

Frequency	TX/RX Port Noise Figure	RX2 Port Noise Figure
< 800 MHz	11.0 dB	10.0 dB
800 MHz - 1.8 GHz	6.5 dB	5.5 dB
1.8 GHz - 2.8 GHz	7.0 dB	6.0 dB
2.8 GHz - 3.8 GHz	7.5 dB	6.5 dB
3.8 GHz - 5.0 GHz	8.5 dB	7.5 dB
5.0 GHz - 6.0 GHz	11.0 dB	10.0 dB

Table 3: RX Noise Figure

Frequency	RX Input Third-Order Intercept (IIP3) (dBm)
450 MHz - 1.0 GHz	> 13 dBm
1.0 GHz - 4.5 GHz	> 17 dBm
4.5 GHz - 6.0 GHz	> 16 dBm

Table 4: RX Input Third-Order Intercept (IIP3) (dBm)

- DDR3 Memory size
    - 2,048 MB (PL)
    - 1,024 MB (PS)

You must use either the Level VI Efficiency power supply provided in the shipping kit, or another UL listed ITE power supply marked ?LPS, with the USRP N320/N321.

- Input voltage: 12 VDC
- Input current: 7.0 A, maximum
- Typical power consumption: 60 W to 75 W, varies by application

- Ettus Research recommends to always use the latest stable version of UHD
- If you need to clean the module, wipe it with a dry towel.

- Current Hardware Revision: A
- Minimum version of UHD required: 3.14.0.0
- Due to product compliance restrictions on products with TPM (Trusted Platform Module) components to a few countries, the USRP N320/N321 is available in two variants:
    - Standard variant with TPM
    - Non-TPM variant

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    - Standard variant with TPM
    - Non-TPM variant

There are three master clock rates (MCR) supported on the N320/N321: 200 MHz, 245.76 MHz, 250 MHz

The sampling rate must be an integer decimation rate of the MCR. Ideally, this decimation factor should be an even number. An odd decimation factor will result in additional unwanted attenuation (roll-off from the CIC filter in the DUC and DDC blocks in the FPGA). The valid decimation rates are between 1 and 1024.

If the desired sampling rate is not directly supported by the hardware, then it will be necessary to re-sample in software. This can be done in C++ using libraries such as Liquid DSP [1], or can be done in GNU Radio, in which there are three blocks that perform sampling rate conversion.

(L × W × H)

- 35.71 cm × 21.11 cm × 4.37 cm
- 14.06 in. × 8.31 in. × 1.72 in.

- 3.13 kg

- Media:cu usrp-n320.pdf

- Media:cu usrp-n321.pdf

- N320 / N321: 0 to 50 °C

- N320 / N321: -40 to 70 °C

- 10% to 90% non-condensing

- Motherboard: File:USRP N3XX MB Schematic.pdf
- Daughterboard: File:N32X Daughterboard Schematic.pdf

- Support GPSDO NMEA Strings

You can query the lock status with the `gps_locked` sensor, as well as obtain raw NMEA sentences using the `gps_gprmc`, and `gps_gpgga` sensors. Location information can be parsed out of the `gps_gpgga` sensor by using `gpsd` or another NMEA parser.

Module Specifications

1 PPS Timing Accuracy from GPS receiver	<8ns to UTC RMS (1-Sigma) GPS Locked
Holdover Stability (1 week with GPS)	<±50us over 3 Hour Period @+25°C (No Motion, No Airflow)
1 PPS Output	3.3VDC CMOS
Serial Port	TTL Level, GPS NMEA Output with 1Hz or 5Hz update rate, Integrated into UHD

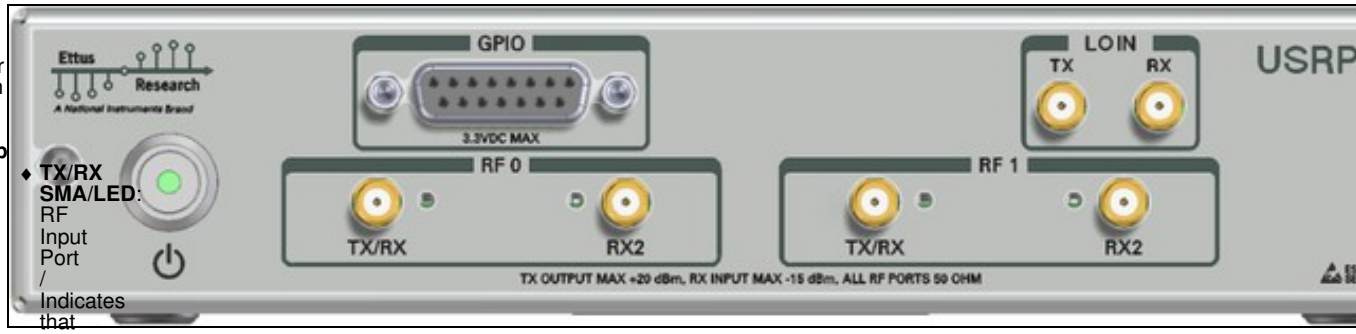
GPS Frequency	L1, C/A 1574MHz
GPS Antenna	Active (3V compatible) or Passive (0dB to +30dB gain)
GPS Receiver	65 Channels, QZSS, SBAS WAAS, EGNOS, MSAS capable Supports Position and Hold over-determined clock mode
Sensitivity	Acquisition -148dBm, Tracking -165dBm
TTFF	Cold Start: <32 sec, Warm Start: 1 sec, Hot Start: 1 sec
ADEV	10s: <7E-011 10Ks: <2E-012 (GPS Locked, 25°C, no motion, no airflow)
Warm Up Time / Stabilization Time	<10 min at +25C to 1E-09 Accuracy
Supply Voltage (Vdd)	3.3V Single-Supply, +0.2V/-0.15V
Power Consumption	<0.16W
Operating Temperature	-10°C to +70°C
Storage Temperature	-45C to 85C

Oscillator Specifications (internal)	
Frequency	20MHz
Output of lock	3Vpp CMOS
Phase Noise crystal	-140 dBc/Hz
20MHz Reference	2E-08 After 1 Hour @ +25°C without GPS
RF Output Amplitude	3Vpp CMOS
20MHz Phase Jitter (100Hz to 10MHz)	<0.135ps rms
Frequency Stability Over Temperature (0°C to +60°C)	+0.1ppm (internal TCXO without GPS)
Warm Up Time	≤ 1 min at +25C
Phase Noise at 20MHz	1Hz -65 dBc/Hz 10Hz -97 dBc/Hz 100Hz -116 dBc/Hz 1kHz -136 dBc/Hz 10kHz <-148 dBc/Hz 100 kHz <-155 dBc/Hz

- Spec Sheet: http://www.jackson-labs.com/assets/uploads/main/LTE-Lite_specsheet_20MHz.pdf
- User Manual: http://www.jackson-labs.com/assets/uploads/main/LTE-Lite.pdf

The Verilog code for the FPGA in the USRP N320/N321 is open-source, and users are free to modify and customize it for their needs. However, certain modifications may result in either bricking the device, or even in physical damage to the unit. Specifically, changing the I/O interface of the FPGA in any way, or modifying the pin and timing constraint files, could result in physical damage to other components on the motherboard, external to the FPGA, and doing this will void the warranty. The constraint files should not be modified. Please note that modifications to the FPGA are made at the risk of the user, and may not be covered by the warranty of the device.

- **PWR**: Power switch
- **RF 0 Group**
  - **TX/RX SMA/LED**: RF Input Port / Indicates that data



is streaming on the TX/RX channel on daughterboard 0, channel 0
    - **RX2 SMA/LED**: RF Input Port / Indicates that data is streaming on the RX2 channel on daughterboard 0, channel 0
- **RF 1 Group**
    - **TX/RX SMA/LED**: RF Input Port / Indicates that data is streaming on the TX/RX channel on daughterboard 1, channel 0.
    - **RX2 SMA/LED**: RF Input Port / Indicates that data is streaming on the RX2 channel on daughterboard 1, channel 0
- **LO IN**
    - **TX**: Input port for TX LO. Supported LO frequency range is from 450 MHz

to
6
GHz.
External
LO
inputs
below
450
MHz
are
not
supported.
The
LO
input
signal
level
should
be
+5
dBm,
but
may
be
between
+3
dBm
and
+7
dBm.

- ♦ **RX**:
Input
port
for
RX
LO
of
Daughterboard
0.
Supported
LO
frequency
range
is
from
450
MHz
to
6
GHz.
External
LO
inputs
below
450
MHz
are
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The
LO
input
signal
level
should
be
+5
dBm,
but
may
be
between
+3
dBm
and
+7
dBm.

- **GPIO**
  - ♦ **GPIO**:
DB15
GPIO
Interface.
Additional
details
below.

- **GPS ANT**: Connection for the GPS antenna
- **REF IN**: Reference clock input
- **PPS/TRIG IN**: Input port for the PPS signal
- **TRIG OUT**: Output port for the exported reference clock
- **PWR**: Connector for the USRP N320 Series power supply
- **RESET**: Input button to reset device
- **MicroSD**: MicroSD Card for OE Linux File System
- **JTAG**: Micro USB connector for the on-board USB-JTAG programmer
- **USB 2.0**: Host USB connector to ARM CPU
- **SFP+**: 1/10Gb SFP+ ports for Ethernet interfaces
- **QSFP+**: QSFP+ port for Ethernet interfaces (2 x 10Gb lanes)
- **10/1000/1000**: 10/100/1000 Mb

Ethernet interface to ARM CPU

The GPIO port is not meant to drive big loads. You should not try to source more than 5mA per pin.

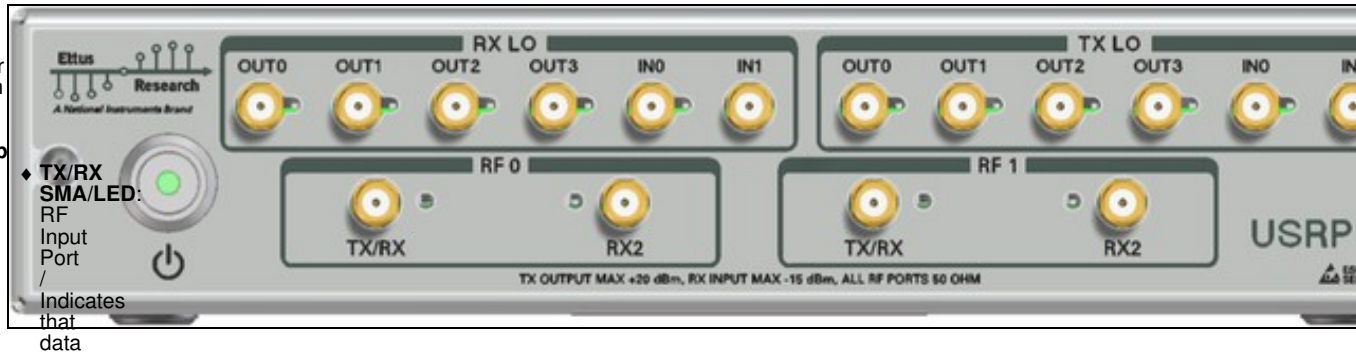
The +3.3V is for ESD clamping purposes only and not designed to deliver high currents.

The hardware power on state and UHD initial state for the front-panel GPIOs is high-Z. For the N320, there are no external pull-ups/pull-downs for the GPIO pins, but the FPGAs do have them and they are configured as follows: pull-down.

- Pin 1: +3.3V
- Pin 2: Data[0]
- Pin 3: Data[1]
- Pin 4: Data[2]
- Pin 5: Data[3]
- Pin 6: Data[4]
- Pin 7: Data[5]
- Pin 8: Data[6]
- Pin 9: Data[7]
- Pin 10: Data[8]
- Pin 11: Data[9]
- Pin 12: Data[10]
- Pin 13: Data[11]
- Pin 14: 0V
- Pin 15: 0V

Note: Please see the E3x0/X3x0/N3x0 GPIO API for information on configuring and using the GPIO bus.

- **PWR**: Power switch
- **RF 0 Group**
  - **TX/RX SMA/LED**: RF Input Port / Indicates that data is streaming on the TX/RX channel on daughterboard 0, channel 0
  - **RX2 SMA/LED**: RF Input Port / Indicates that data is streaming on the RX2 channel on daughterboard 0, channel 0



- **RF 1 Group**
  - **TX/RX SMA/LED**: RF Input Port /

Indicates that data is streaming on the TX/RX channel on daughterboard 1, channel 0.

- **RX2 SMA/LED**: RF Input Port / Indicates that data is streaming on the RX2 channel on daughterboard 1, channel 0

- **TX LO**
  - **IN0**: Input port for TX LO. Supported LO frequency range is from 450 MHz to 6 GHz. External LO inputs below 450 MHz are not supported. The LO input signal level should be +5 dBm, but may be between +3 dBm and +7 dBm.
  - **IN1**: Input port for TX LO. Supported LO frequency range

is from 450 MHz to 6 GHz. External LO inputs below 450 MHz are not supported. The LO input signal level should be +5 dBm, but may be between +3 dBm and +7 dBm.
- **OUT0-3**: TX LO Outputs from 1:4 splitter

- **RX LO**
  - **IN0**: Input port for RX LO of Daughterboard 0. Supported LO frequency range is from 450 MHz to 6 GHz. External LO inputs below 450 MHz are not supported. The LO input signal level should be +5 dBm, but may be between +3 dBm and +7 dBm.

- **IN1**: Input port for RX LO of Daughterboard 0. Supported LO frequency range is from 450 MHz to 6 GHz. External LO inputs below 450 MHz are not supported. The LO input signal level should be +5 dBm, but may be between +3 dBm and +7 dBm.
- **OUT0-3**: RX LO Outputs from 1:4 splitter

- Additional details on the N321 Distribution Board can be found here: https://files.ettus.com/manual/page_usrp_n3xx.html#n3xx_rh_lo_sharing

- **GPS ANT**: Connection for the GPS antenna
- **REF IN**: Reference clock input
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Using an external 10 MHz reference clock, a square wave will offer the best phase noise performance, but a sinusoidal is acceptable. The power level of the reference clock cannot exceed +10 dBm.

Using a PPS signal for timestamp synchronization requires a square wave signal with the following a 5Vpp amplitude.

To test the PPS input, you can use the following tool from the UHD examples:

- `<args>` are device address arguments (optional if only one USRP device is on your machine)

```
cd <install-path>/lib/uhd/examples ./test_pps_input ?args=<args>
```

As of December 1st, 2010 all Ettus Research products are RoHS compliant unless otherwise noted. More information can be found at http://ettus.com/legal/rohs-information

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Chinese Customers

National Instruments is in compliance with the Chinese policy on the Restriction of Hazardous Substances (RoHS) used in Electronic Information Products. For more information about the National Instruments China RoHS compliance, visit ni.com/environment/rohs_china.

FPGA Resources

UHD Stable Binaries

UHD Source Code on Github

Recommended 10 Gigabit Ethernet Cards

- Intel X520-DA2
  - Intel® Ethernet Converged Network Adapter X520-DA2
- Intel X520-DA1
  - Intel® Ethernet Converged Network Adapter X520-DA1
- Intel X710-DA2
  - Intel® Ethernet Converged Network Adapter X710-DA2
- Intel X710-DA4
  - Intel® Ethernet Converged Network Adapter X710-DA4
- Mellanox MCX4121A-ACAT
  - Mellanox MCX4121A-ACAT

The power supply provided with the USRP N320 kit is packaged with a power cord that is compatible with power outlets in the US/Japan. If you are not using the USRP N320 in the US/Japan, we recommend purchasing the International USRP N320 Power Cord set.

Ettus Research currently offers direct-connect, copper cabling accessories for the USRP N320/N321. However, it is also possible to use multi-mode fiber instead of copper connections for these devices. In this section, we will provide general guidance on the types of fiber adapters and cables that can be used with these products.

The USRP N320/N321 USRP is compatible with most brands of SFP+ fiber adapters. In some cases, other equipment in the systems such as 1/10 Gigabit Ethernet switches are only compatible with specific brands of SFP+ adapters and cables. As a general rule, we recommend checking compatibility with the switches and network cards in your system before purchasing an adapter.

Ettus Research does test the USRP N320/N321 USRP devices with our 10 Gigabit Ethernet Connectivity Kit and a Blade Networks G8124 1/10 GigE switch. Here are is a list of known-good cables and adapters.

Ettus Research has only tested multi-mode fiber accessories.

- Approved Optics BN-CKM-SP-SR-A
- Elpeus 10GbE SFP+ AOC Cable, 3 meters

Many new motherboards come equipped with an onboard 10Gb RJ45 NIC. It is possible to use a SFP+ to RJ45 adapter and operate at 10Gb speeds using a Cat6/7 Ethernet cables.

Ettus Research has tested the adapters linked below.

- 10Gtek SFP+ to RJ45 Copper Module
- ProLabs 10G-SFPP-T-C