X310

Contents

The Ettus Research USRP X310 is a high-performance, scalable software defined radio (SDR) platform for designing and deploying next generation wireless communications systems. The hardware architecture combines two extended-bandwidth daughterboard slots covering DC ? 6 GHz with up to 160 MHz of baseband bandwidth, multiple high-speed interface options (PCIe, dual 10 GigE, dual 1 GigE), and a large user-programmable Kintex-7 FPGA in a convenient desktop or rack-mountable half-wide 1U form factor.

- Xilinx Kintex-7 XC7K325T FPGA
- 14 bit 200 MS/s ADC
- 16 bit 800 MS/s DAC
- Frequency range: DC - 6 GHz with suitable daughterboard
- Up 160MHz bandwidth per channel
- Two wide-bandwidth RF daughterboard slots
- Optional GPSDO
- Multiple high-speed interfaces (Dual 10G, PCIe Express, ExpressCard, Dual 1G)

- Xilinx Kintex-7 XC7K410T FPGA
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- WBX-120 / WBX-40
- SBX-120 / SBX-40
- CBX-120 / CBX-40
- UBX-160 / UBX-40
- BasicTX / BasicRX
- LFRX / LFTX
- TwinRX
- DBSRX2 (EOL)
- RFX Series (EOL)
- TVRX2 (EOL)

- SSB/LO Suppression -35/50 dBc
- Phase Noise 3.5 GHz 1.0 deg RMS
- Phase Noise 6 GHz 1.5 deg RMS
- Power Output >10dBm
- IIP3 (@ typ NF) 0dBm
- Typical Noise Figure 8dB

- Ettus Research recommends to always use the latest stable version of UHD

- Current Hardware Revision: 8
- Minimum version of UHD required: 3.9.0

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There are two master clock rates (MCR) supported on the X300 and X310: 200.0 MHz and 184.32 MHz.

The sampling rate must be an integer decimation rate of the MCR. Ideally, this decimation factor should be an even number. An odd decimation factor will result in additional unwanted attenuation (roll-off from the CIC filter in the DUC and DDC blocks in the FPGA). The valid decimation rates are between 1 and 1024.

For the MCR of 200.0 MHz, the achievable sampling rates using an even decimation factor are 200.0, 100.0, 50.0, 33.33, 25.0, 20.0, 16.67, 14.286 Msps, ... 195.31 Ksps.

For the MCR of 184.32 MHz, the achievable sampling rates using an even decimation factor are 184.32, 92.16, 46.08, 30.72, 23.04, 18.432, 15.36, 13.166 Msps, ... 180.0 Ksps.

If the desired sampling rate is not directly supported by the hardware, then it will be necessary to re-sample in software. This can be done in C++ using libraries such as Liquid DSP [1], or can be done in GNU Radio, in which there are three blocks that perform sampling rate conversion.

27.7 x 21.8 x 3.9 cm

With 2x SBX-120: 1.7kg

- Enclosure
- Motherboard
- Rackmount kit

- Motherboard

- Enclosure

- X300/X310: 25 °C

- 10% to 90% non-condensing

X300/X310 Schematics

Part Number	Description	Schematic ID (Page)
XC7K325T / XC7K410T	FPGA	U23 (3,5,8,9,10,18)
AD9146	Dual Channel, 16-Bit, 1230 MSPS DAC	U12, U36 (7)
ADS62P48	Dual Channel, 14-Bit 210 MSPS ADC	U11, U35 (6)
FIN1002	High Speed Differential Receiver	U3, U5, U31, U32 (4)
24LC256T	EEPROM	U530 (11)
LMK04816BISQ/NOPB_1/3	Jitter Cleaner With Dual Loop PLLs	U531 (11)
SY89547LMGTR	Multiplexer	U506 (12)
SN74AUP1T17	Single Schmitt-Trigger Buffer Gate	U6, U519 (12)
TPS54620RGYT	Synchronous Step Down SWIFT? Converter	U515 (21); U516 (26)
LT1764EQ-3.3	Voltage Regulator	U27 (21); U516 (26)
TPS7A47	Voltage Regulator	U28, U532 (21)
LTC3603EUF_TRPBF	Monolithic Synchronous Step-Down Regulator	U517 (23); U500 (25); U514, U513 (27)
TPS77625_SM	Low-Dropout Voltage Regulators	U30 (23)
TPS79318_SM	Low-Dropout Voltage Regulators	U510 (27)
OSC-96MHZ-724821-01	Voltage Controlled Crystal Oscillator	U25 (11)

- Support GPSDO NMEA Strings
- JacksonLabs LC_XO

You can query the lock status with the `gps_locked` sensor, as well as obtain raw NMEA sentences using the `gps_gprmc`, and `gps_gpgga` sensors. Location information can be parsed out of the `gps_gpgga` sensor by using `gpsd` or another NMEA parser.

- Utilization statistics are subject to change between UHD releases. This information is current as of UHD 3.9.4 and was taken directly from Xilinx Vivado 2014.4.

```
1. Slice Logic
--------------

+----------------------------+-------+-----------+-------+
|          Site Type         |  Used | Available | Util% |
+----------------------------+-------+-----------+-------+
| Slice LUTs                 | 61622 |    203800 | 30.23 |
|   LUT as Logic             | 52887 |    203800 | 25.95 |
|   LUT as Memory            |  8735 |     64000 | 13.64 |
|     LUT as Distributed RAM |  1878 |           |       |
|     LUT as Shift Register  |  6857 |           |       |
| Slice Registers            | 62961 |    407600 | 15.44 |
|   Register as Flip Flop    | 62961 |    407600 | 15.44 |
|   Register as Latch        |     0 |    407600 |  0.00 |
| F7 Muxes                   |  1209 |    101900 |  1.18 |
| F8 Muxes                   |   150 |     50950 |  0.29 |
+----------------------------+-------+-----------+-------+

3. Memory
```

Site Type	Used	Available	Util%
Block RAM Tile	409	445	91.91
RAMB36/FIFO*	398	445	89.43
RAMB36E1 only	398		
RAMB18	22	890	2.47
RAMB18E1 only	22		

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a

4. DSP

Site Type	Used	Available	Util%
DSPs	123	840	14.64
DSP48E1 only	123		

1. Slice Logic

Site Type	Used	Available	Util%
Slice LUTs	61616	254200	24.23
LUT as Logic	52885	254200	20.80
LUT as Memory	8731	90600	9.63
LUT as Distributed RAM	1878		
LUT as Shift Register	6853		
Slice Registers	62958	508400	12.38
Register as Flip Flop	62958	508400	12.38
Register as Latch	0	508400	0.00
F7 Muxes	1209	127100	0.95
F8 Muxes	150	63550	0.23

3. Memory

Site Type	Used	Available	Util%
Block RAM Tile	409	795	51.44
RAMB36/FIFO*	398	795	50.06
RAMB36E1 only	398		
RAMB18	22	1590	1.38
RAMB18E1 only	22		

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a

4. DSP

Site Type	Used	Available	Util%
DSPs	123	1540	7.98
DSP48E1 only	123		

The Verilog code for the FPGA in the USRP X300 and USRP X310 is open-source, and users are free to modify and customize it for their needs. However, certain modifications may result in either bricking the device, or even in physical damage to the unit. Specifically, changing the I/O interface of the FPGA in any way (do not remove any of the I/O for the PCIe interface, such as `x300_pcie_int` and `LvFpga_Chinch_Interface`), or modifying the pin and timing constraint files, could result in physical damage to other components on the motherboard, external to the FPGA, and doing this will void the warranty. Also, even if the PCIe interface is not being used, you cannot remove or reassign these pins in the constraint file. The constraint files should not be modified. Please note that modifications to the FPGA are made at the risk of the user, and may not be covered by the warranty of the device.

The USRP X300 series runs a small amount of software within the FPGA, within a ZPU soft processor. Its main responsibility is to provide access to some registers, handle the networking stacks, and monitor the USRP status.

The source code for the ZPU is stored in `firmware/usrp3/` in the UHD repository. To modify the firmware, you need to download a recent ZPU compiler (e.g. from https://github.com/zylin/zpugcc/tree/master/releases/20150428). Unpack the tarball (e.g., into `/usr/local`) and make sure the `zpu-elf-gcc` binary is in your path. Then, execute the following steps:

- Create and enter a build directory: `mkdir build && cd build`
- Run cmake: `cmake /path/to/firmware/usrp3/`
    - ♦ If all is correctly configured, and the ZPU compiler can be found, this will pass without errors.
- Build the firmware: `make`
    - ♦ This should yield output similar to this:

```
Scanning dependencies of target x300
[ 79%] Generating x300_main.map
[ 83%] Generating x300_main.bin
[ 87%] Generating x300_main.ihx
[ 91%] Generating x300_main.dump
[ 95%] Generating x300_main.rom
[100%] Generating x300_main.coe
```

```
[100%] Built target x300
```

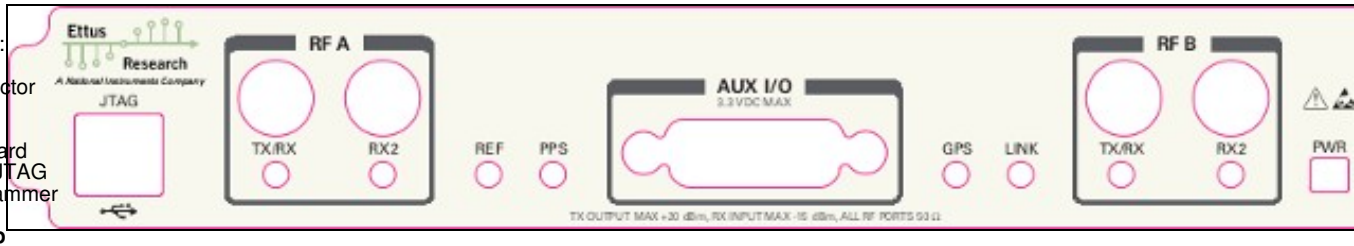
- These files will be copied into the `build/x310` directory.
- To non-persistently load the newly built firmware image into the running FPGA image, simply launch a UHD session with the `fw` parameter. The binary must be within UHD's image dir, e.g. by copying x300_main.bin to the default image directory (e.g., `/usr/local/share/uhd/images`) or by temporarily setting the `UHD_IMAGES_DIR` variable:

```
UHD_IMAGES_DIR=/path/to/build/x300 uhd_usrp_probe --args type=x300,fw=x300_main.bin
```

- To permanently bake the firmware image into the FPGA bitfile, copy the file `x300_main.coe` to `fpga/usrp3/top/x300/ip/bootram/bootram.coe` and rebuild the bitfile.

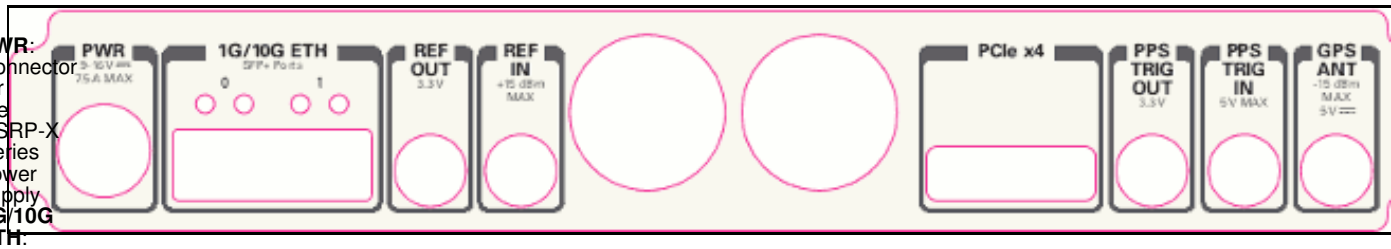
Follow the links below for additional information on configuring each interface for the USRP X300 or X310 SDRs.

- Dual 10 Gigabit Ethernet - 200 MS/s Full Duplex @ 16-bit
- PCIe Express (Desktop) - 200 MS/s Full Duplex @ 16-bit
- ExpressCard (Laptop) - 50 MS/s Full Duplex @ 16-bit
- Dual 1 Gigabit Ethernet - 25 MS/s Full Duplex @ 16-bit



- **JTAG**: USB connector for the on-board USB-JTAG programmer
- **RF A Group**
  - **TX/RX LED**: Indicates that data is streaming on the TX/RX channel on daughterboard A
  - **RX2 LED**: Indicates that data is streaming on the RX2 channel on daughterboard A
- **REF**: Indicates that the external Reference Clock is locked
- **PPS**: Indicates a valid PPS signal by pulsing once per second
- **AUX I/O**: Front panel GPIO connector.
- **GPS**: Indicates that GPS reference

is locked
- **LINK**: Indicates that the host computer is communicating with the device (Activity)
- **RF B Group**
  - **TX/RX LED**: Indicates that data is streaming on the TX/RX channel on daughterboard B
  - **RX2 LED**: Indicates that data is streaming on the RX2 channel on daughterboard B
- **PWR**: Power switch



- **PWR**: Connector for the USRP-X Series power supply
- **1G/10G ETH**: SFP+ ports for Ethernet interfaces
- **REF OUT**: Output port for the exported reference clock
- **REF IN**: Reference clock input
- **PCIe x4**: Connector for Cabled PCI Express link
- **PPS/TRIG OUT**: Output

port for the PPS signal
- **PPS/TRIG IN**: Input port for the PPS signal
- **GPS**: Connection for the GPS antenna

Using an external 10 MHz reference clock, a square wave will offer the best phase noise performance, but a sinusoid is acceptable. The power level of the reference clock cannot exceed +15 dBm.

Using a PPS signal for timestamp synchronization requires a square wave signal with the following a 5Vpp amplitude.

To test the PPS input, you can use the following tool from the UHD examples:

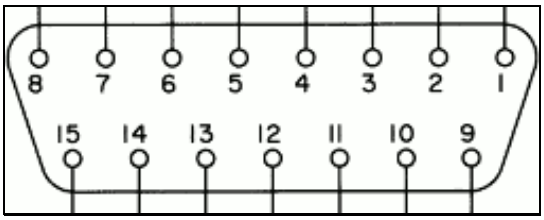
- `<args>` are device address arguments (optional if only one USRP device is on your machine)

```
cd <install-path>/lib/uhd/examples ./test_pps_input ?args=<args>
```

The GPIO port is not meant to drive big loads. You should not try to source more than 5mA per pin.

The +3.3V is for ESD clamping purposes only and not designed to deliver high currents.

The switching speed is below 10 MHz.



The hardware power on state and UHD initial state for the front-panel GPIOs is high-Z. For the X3xx, there are no external pull-ups/pull-downs for the GPIO pins, but the FPGAs do have them and they are configured as follows: X3xx: pull-down.

- Pin 1: +3.3V
- Pin 2: Data[0]
- Pin 3: Data[1]
- Pin 4: Data[2]
- Pin 5: Data[3]
- Pin 6: Data[4]
- Pin 7: Data[5]
- Pin 8: Data[6]
- Pin 9: Data[7]
- Pin 10: Data[8]
- Pin 11: Data[9]
- Pin 12: Data[10]
- Pin 13: Data[11]
- Pin 14: 0V
- Pin 15: 0V

Note: Please see the E3x0/X3x0 GPIO API for information on configuring and using the GPIO bus.

LED	Detail	Description
DS1	1.2V	Power
DS2	TXRX1	Red: TX, Green: RX
DS3	RX1	Green: RX
DS4	REF	Reference Lock
DS5	PPS	Flashes on Edge
DS6	GPS	GPS Lock
DS7	SFP0	Link, Right, Green
DS8	SFP0	Link Activity, Left, Yellow
DS10	TXRX2	Red: TX Green: RX
DS11	RX2	Green: RX
DS12	6V	Daughterboard Power
DS13	3.8V	Power

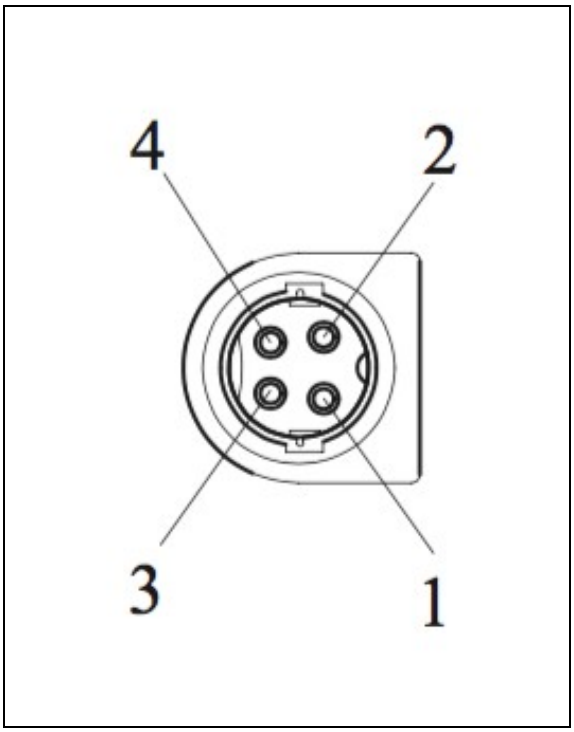
DS14	3.3V	Management Power
DS15	3.3V	Auxiliary Management Power
DS16	3.3V	FPGA Power
DS19	SFP1	Link Active, Left, Yellow
DS20	SFP1	Link, Right, Green
DS21	LINK	Link Activity

Model: PDP-40 by CUI Inc.

Power plug connectors for custom power harnesses can be purchased here:
https://www.digikey.com/products/en?KeyWords=CP-7340-ND&WT.z_cid=sp_102_buynow

Assembly instructions: Media:pdp-40.pdf

- Pins #1 / #2: 12v
- Pins #3 / #4: Ground



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http://ettus.com/legal/rohs-information

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Found on the NI Product Certifications lookup tool here.

FPGA Resources

UHD Stable Binaries

UHD Source Code on Github

In terms of host bandwidth, interface options, and all other hardware features the USRP X300 and USRP 310 are identical. However, the USRP X310 provides a larger FPGA, a Xilinx XC7K410T, as opposed to XC7K325T. While both options provide a significant amount of free resources for custom FPGA development, the XC7K410T provides additional design margin, which translates to ease of development and future expandability. Most users choose the USRP X310 for their development.

USRP X300 and X310 FPGA Resource Summary

Resource Type	USRP X300 (XC7K325T) Count	USRP X310 (XC7K410T) Count
DSP48 Blocks	840	1540
Block Rams (18kB)	890	1590

Logic Cells	326,080	406,720
Slices (logic)	50,950	63,550

For up-to-date information on FPGA resource utilization in the stock FPGA design, please see "USRP 300/X310 FPGA Resources" in the Ettus Research knowledge base (https://kb.ettus.com).

With the increased sample rates used by the USRP X300 and USRP X310, these new device can support extended-bandwidth daughterboards. The WBX-120, SBX-120, and CBX-120 are recommended to take advantage of the full bandwidth capability of the USRP X300 and X310. The WBX-120, SBX-120, and CBX-120 have been upgraded from their predecessors (40 MHz) to use 120 MHz baseband filters. You can select your daughterboard based on the center frequency of your primary application.

Daughterboard	Frequency Range	Bandwidth
WBX-120	50 MHz - 2200 MHz	120 MHz
SBX-120	400 MHz - 4400 MHz	120 MHz
CBX-120	1200 MHz - 6000 MHz	120 MHz
UBX-160	10 MHz - 6000 MHz	160 MHz
TwinRX	10 MHz - 6000 MHz	80 MHz per channel, 160 MHz total

If your application is in the HF frequency range, the LFRX and LFTX are recommended for up to 30 MHz of bandwidth per channel. The BasicRX and BasicTX are ideal for configurations that use an external frontend for tuning and filtering with either an IF or baseband interface.

The USRP X300 and X310 are backward compatible with legacy daughterboards except for the RFX Series and XCVR2450. Please note, while there are two daughterboard slots, the USRP X300/X310 can only support a single TVRX2.

If you plan to transmit or receive over the air, you should also purchase an antenna.

The USRP X300/X310 provide three interface options ? 1 Gigabit Ethernet (1 GigE), 10 Gigabit Ethernet (10 GigE), and PCI-Express (PCIe). The PCIe interface is always available regardless of what FPGA image is loaded. Ettus ships two FPGA image variants, the HG or HGS image which has one 1 GigE interfaces and one 10 GigE interfaces, and the XG image which has two 10 GigE interfaces. Generally, Ettus Research recommends using 10 GigE to achieve the maximum throughput available from the USRP X300/X310. PCIe is recommended for applications that require the lowest possible latency, which is a desirable characteristic for PHY/MAC research. If your application does not require the full bandwidth of the USRP ? X300 and X310, the 1 GigE interface serves as a cost-effective fall-back option. Ettus Research provides a complete interface kit for each of these options, which is also shown in Table 3.

Table 3 - Interface Performance Summary

Interface	Throughput (MS/s @ 16-bit)	Target	Recommended Kit
1 Gigabit	25 MS/s	Desktop/Laptop	Components provided with USRP X300/X310 kit. For additional connections, purchase the following: SFP Adapter + GigE Cable
10 Gigabit	200 MS/s	Desktop	10 GigE Interface Kit
PCI-Express (PCIe, 4 lane)	200 MS/S	Desktop	PCI-Express Desktop Kit
Express Card (PCIe, 1 lane)	50 MS/s	Laptop	ExpressCard Kit

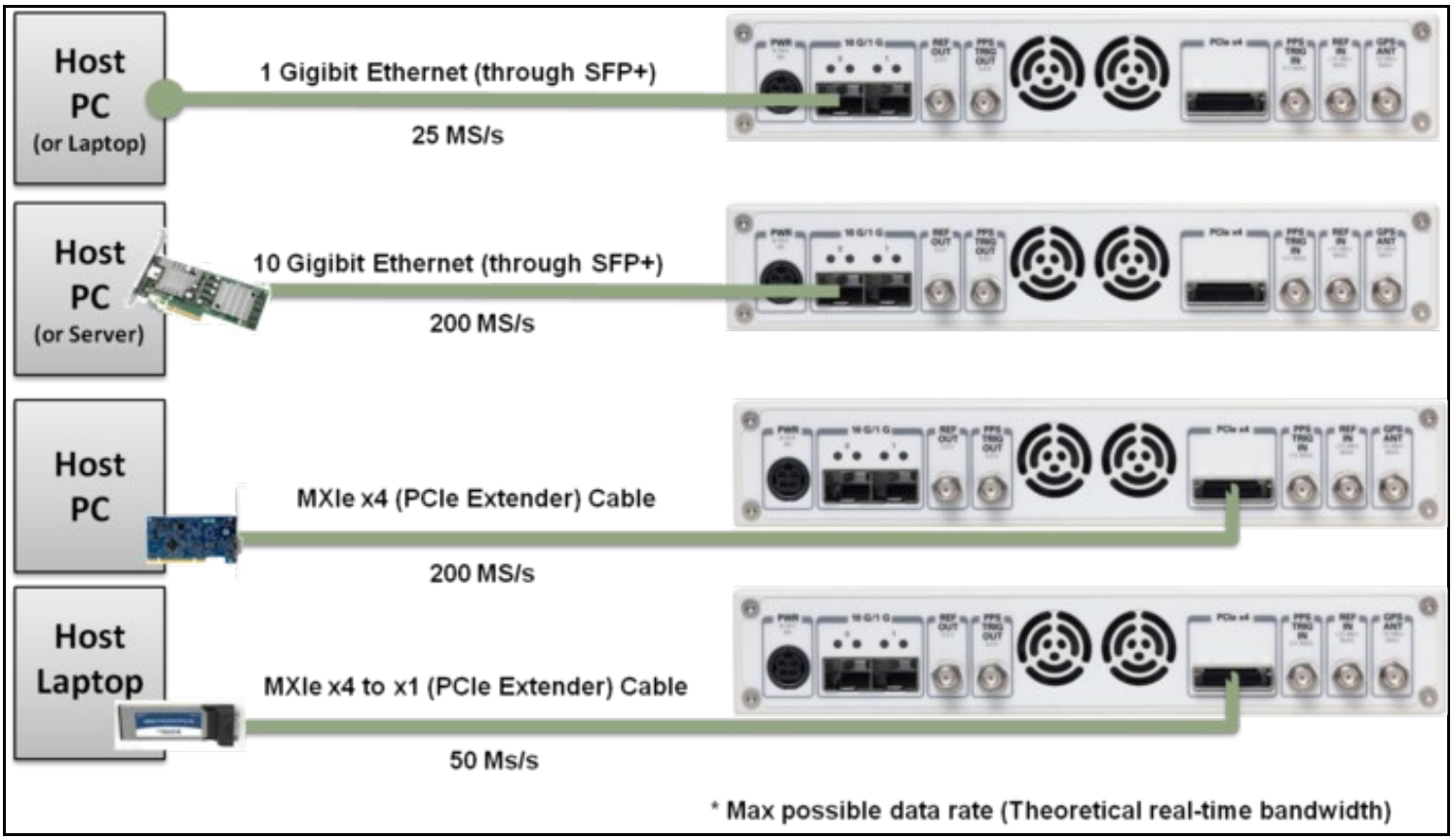

Figure 2 - Host Interface Options

See this app note for how to use the X3x0 with dual 10 GbE links.

Recommended 10 Gigabit Ethernet Cards

- Intel X520-DA2
  - Intel® Ethernet Converged Network Adapter X520-DA2
- Intel X520-DA1
  - Intel® Ethernet Converged Network Adapter X520-DA1
- Intel X710-DA2
  - Intel® Ethernet Converged Network Adapter X710-DA2
- Intel X710-DA4
  - Intel® Ethernet Converged Network Adapter X710-DA4
- Mellanox MCX4121A-ACAT
  - Mellanox MCX4121A-ACAT

The power supply provided with the USRP X300/X310 kit is packaged with a power cord that is compatible with power outlets in the US/Japan. If you are not using the USRP X300/X310 in the US/Japan, we recommend purchasing the International USRP X300/X310 Power Cord set.

The USRP X300 and USRP X310 provide the option to integrate a high-accuracy GPS-disciplined oscillator (GPSDO). The GPSDO improves the accuracy of the internal frequency reference to 20 ppb, or 0.1 ppb if the GPS is synchronized to the GPS constellation. When synchronized to the GPS constellation, all USRP ? devices will also be synchronized in time within 50 ns.

	Internal TCXO	**GPS-Disciplined Clock**
Frequency Reference	TCXO	OCXO
Frequency Accuracy (unlocked)	± 2.5ppm ± 2,500 Hz @ 1 GHz	± 25 ppb ± 25 Hz @ 1 GHz
Frequency Accuracy (GPS-Disciplined)		± 0.01ppb ~ ± 0.01 Hz @ 1 GHz
GPS Time Sync Accuracy		±50ns to UTC Time**
10 MHz Reference Phase Drift with GPS Sync		<±20ns After 1 Hour**

The GPSDO Mini Kit will improve the accuracy of the USRP reference clock, even if it does not receive signals from the GPS Constellation. However, to achieve the best accuracy possible, and to achieve global timing alignment across multiple USRPs, Ettus Research recommends the GPSDO Mini Antenna Kit.

The USRP X300 and X310 include a DB15 connector on the front panel that provides convenient access to GPIO signals. Each pin can be configured as an input or output, uses 3.3V-level logic, and is protected with basic anti-static circuitry. These pins can be used to control external devices like RF switches and amplifiers, trigger software events on the host, or even provide basic debugging functionality. The USRP GPIO Kit is an affordable option that provides access to these signals with a DB15 cable and a breakout board. The breakout board allows the user to connect external devices through a terminal block. The user can also solder wires and components into the dedicated prototyping area.

Multiple USRP X300/X310s can be synchronized for coherent operation by sharing a common 10 MHz and 1 PPS signal. We recommend using a star-distribution topology with an OctoClock or OctoClock-G, as seen in Figure 4. This requires matched length cables to be used for both 10 MHz and 1 PPS.

For more information about MIMO operation, please see the MIMO and Synchronization Application Note.

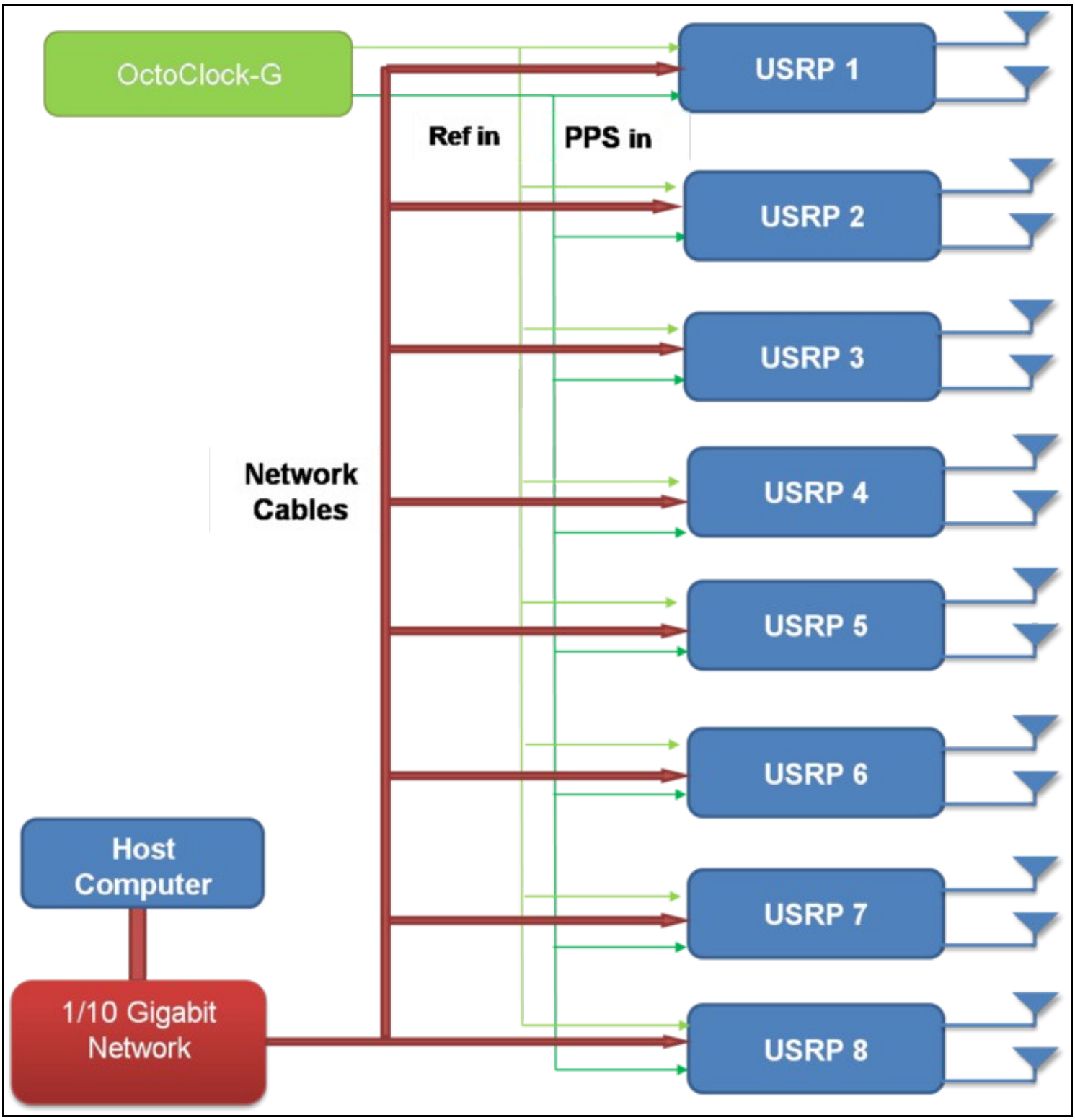

Figure 4 - Star-Distribution of 10 MHz/PPS Signals with OctoClock

The USRP X300 and X310 were designed to be used with a 1U Rackmount Assembly for building high-density MIMO systems in a compact and well-organized setup. This mount supports one or two compatible USRPs, and if two are mounted then there are rubber standoffs between the USRPs to avoid both direct contact and surface scratching. If the user will be developing in a laboratory environment or building a high-channel count USRP

system, then a 1U Rackmount Assembly is highly recommended. This specific mount is compatible with only the USRP X300 and X310, and allows the integration of up to four bidirectional -- or eight receive-only -- RF channels per 1U.

Ettus Research currently offers direct-connect, copper cabling accessories for the USRP X300 and USRP X310. However, it is also possible to use multi-mode fiber instead of copper connections for these devices.

The USRP X Series is compatible with most brands of SFP+ fiber adapters. In some cases, other equipment in the systems such as 1/10 Gigabith Ethernet switches are only compatible with specific brands of SFP+ adapters and cables. As a general rule, we recommend checking compatibility with the switches and network cards in your system before purchasing an adapter.

Ettus Research does test the USRP X Series devices with our 10 Gigabit Ethernet Connectivity Kit and a Blade Networks G8124 1/10 GigE switch. Here are is a list of known-good cables and adapters.

Ettus Research has only tested multi-mode fiber accessories.

- Approved Optics Blade Networks BN-CKM-SP-SR-A
- Myricom Fiber Cables for 10GBase-SR, 3 Meters 10G-SR-3M

Many new motherboards come equipped with an onboard 10Gb RJ45 NIC. It is possible to use a SFP+ to RJ45 adapter and operate at 10Gb speeds using a Cat6/7 Ethernet cables.

Ettus Research has tested the adapters linked below.

- 10Gtek SFP+ to RJ45 Copper Module
- ProLabs 10G-SFPP-T-C

USRP? X300 and USRP? X310 SDRs Frequently Asked Questions

- **What is the bandwidth of the USRP X300/X310**

The ADC rate on each analog RX channel is 200 MS/s quadrature, which provides a theoretical analog bandwidth of approximately 80% of the Nyquist bandwidth of +/- 100 MHz (+/- 80 MHz around the center frequency). The resulting maximum theoretical analog bandwidth is 160 MHz. The actual analog bandwidth may be reduced due the RF daughterboard selected.

RF Daughterboard Bandwidths: See the daughterboard specifications [link]

FPGA Processing Bandwidth: Up to 200 MS/s quadrature.

Host Bandwidth: Up to 200 MS/s quadrature, dependent on selected interface

For more information about achieving the maximum bandwidth with a USRP X300/X310, please see the "USRP X300/X310 Configuration Guide" or the "USRP System Bandwidth" application note.

- **How can I program the USRP X300/X310**

Like all other USRP models, the USRP X300 and X310 are compatible with the USRP Hardware Driver? (UHD) architecture. The UHD architecture is a common driver that allows users to develop and execute applications on a host-PC. UHD provides a direct C++ API to control and stream to/from the USRP X300/X310. It also provides compatibility with a variety of third-party software frameworks including GNU Radio, LabVIEW, and Matlab. You may also customize the FPGA image provided with UHD to integrate your own signal processing. For more information about UHD, and supported software frameworks, please see:

http://files.ettus.com/manual/

- **How do I update the FPGA images and firmware with the latest from UHD**

You can find more information about updating the FPGA image in the UHD manual:
https://files.ettus.com/manual/page_usrp_x3x0.html#x3x0_getting_started_fpga_update

- **How can I modify the FPGA of the USRP X300/X310**

The source code (Verilog) for the USRP X300/X310 is available in the UHD repository. The build process leverages the existing CMAKE build system used to compile the host-side driver. A Linux-based setup will provide the best results.

Which FPGA toolchain required to build the FPGA images will depend upon your version of UHD. For more details please see the UHD Software Resource page.

- **How much free space is available in the USRP X300/X310 FPGA**

Please see the USRP X300/X310 FPGA resources page for more information.

- **What type of PC setup is recommended for use with the USRP X300/X310**

The type of PC required depends heavily on the complexity and bandwidth of the application. To demonstrate the USRP X300/X310, we typically use a desktop computer with a quadcore i7, 8+ GB of DDR3, and install the PCIe interface card that is also provide with the 10 GigE, PCIe, and ExpressCard interface kits.

- **What frequency range does the USRP X300/X310 cover**

The frequency range depends on the daughterboard select by the users. For more information, please see the USRP X300/X310 Configuration Guide.

- **What components do I need to purchase for a complete USRP X300/X310 system**

For a more comprehensive guide, please see the USRP X300/X310 Configuration Guide.

- **What is the difference between the USRP X300/X310**

The USRP X310 includes a larger Kintex-7 series FPGA (XC7K410T) with additional development resources for more complex designs. The USRP X300 includes the smaller XC7K325T FPGA.

- **What is the part number of the X300/X310 power connector**

Model: PDP-40 by CUI Inc. Power plug connectors for custom power harnesses can be purchased here:
https://www.digikey.com/products/en?KeyWords=CP-7340-ND&WT.z_cid=sp_102_buynow